9397 168 80142

1. GENERAL INFORMATION

This introduction describes a novel two channel passive infrared (PIR) movement sensing system comprising a RPY222 interdigitated sensor and pattern recognition signal processing circuitry.

The characteristics of the overall system provide reliable detection with excellent false trigger immunity.

The effects of potential false trigger sources including changing ambient temperature, thermal disturbances, random noise spikes and interference are shown to be greatly reduced.

Currently the vast majority of passive infrared movement sensing units are single-channel systems employing compensated dual element sensors such as the RPW100/KRX10. The false trigger performance of these systems is essentially determined by the level of incidence of internally and externally generated random noise spike phenomena. These unwanted events can be effectively eliminated by using two identical channels in parallel to provide more information. Since the probability of random events occurring simultaneously in both channels is extremely low, the overall performance can be substantially improved.

A suitable sensor is our RPY222 which comprises two separate series-connected dual element sensors (Fig.1) in a single 4 lead TO-39 encapsulation. The interdigitated electrode construction (Patent No. GB 2170952A) has been designed so as to provide almost coincident signals from each channel to give further options in the design of the associated signal processing (Patent No. GB 217424A).

2. PIR INTRUDER ALARM SYSTEMS

A block diagram of a simple passive infrared intruder alarm system is shown in Fig.2. It basically consists of:

a. A Fresnel lens array.
b. A PIR sensor
c. Two gain stages using bandpass amplifiers.
d. A window comparator determined by positive and negative thresholds.
e. A logic circuit to perform simple signal processing techniques, as discussed below.
f. An alarm relay and output.

2.1 FRONT END CIRCUIT DESIGN

A circuit suitable for use with our Fresnel lens array and a single-channel sensor is shown in Fig.3.

The amplifier frequency response requirements are defined by the range and speed of the intruder, the frequency characteristics of the sensor and the zone dimensions of the associated Fresnel optics.

These factors have been taken into account in the design to give optimum performance. The sensor is operated in a source follower configuration and followed by two operational amplifier gain stages which provide 66 dB of gain and defined 3 dB bandwidth of 0.5 Hz to 5 Hz. Table 1 lists the component values that give the above frequency response and gain characteristics.

The window comparator threshold levels of +0.5 V and −0.5 V are established by the potential divider chain formed by the resistor network R8, R9 and R10. When the input signal exceeds these preset levels the appropriate comparator switches from a LOW to a HIGH state.

Resistor	Value (Ω)
R1	1 M2
R2	820 k
R3	4 k7
R4	120 k
R5	120 k
R6	120 k
R7	3 M3
R8	56 k
R9	27 k
R10	56 k
R11	56 k
R12	100 k

Capacitor	Value
C1	22 μF
C2	100 nF
C3	10 μF
C4	10 μF
C5	2.2 nF
C6	10 μF
C7	1 μF
C8	10 nF

Table 1

In a two channel unit this circuitry has to be duplicated to provide two completely independent signal paths with the four outputs corresponding to +A, −A, +B and −B.

2.2 SIGNAL PROCESSING TECHNIQUES FOR SINGLE CHANNEL SYSTEMS

Three principal techniques are currently used for processing output signals from the 'front end' comparators:

a. Single-shot signal processing.
b. Dual-polarity signal processing.
c. Pulse-count signal processing.

a. Single-shot signal processing

This option can be easily implemented by logically combining the comparator outputs to give an alarm condition when either the positive OR the negative threshold level comparator switches from a LOW to HIGH state. The technique can be prone to false triggers due to electrical noise in the 'front end' circuitry, thermal effects and external factors such as radio frequency interference.

b. Dual-polarity signal processing

This technique relies on the fact that an intruder traversing a zone will generate a dual polarity signal with a characteristic time between peaks. Following a comparator transition the corresponding output is held high for a set time period. Both outputs are connected to the inputs of an AND gate and an alarm condition initiated when both inputs are simultaneously HIGH. To some extent this method reduces the problems associated with single-shot signal processing, but electrical, thermal and external disturbances often give rise to dual-polarity signals.

c. Pulse-count signal processing

This system will count N comparator output pulses within a predetermined time period before raising an alarm condition. The number of pulses, N, to give optimum performance is a function of the zone coverage and the associated optics. False triggers due to non-intruder type disturbances are now greatly improved but an intruder with knowledge of the detector unit employed could defeat the system.

3. TWO-CHANNEL SIGNAL PROCESSING

Present two-channel detection systems generate an alarm condition in response to the occurrence of an electrical output on both channels within a predetermined period of time. For increased false trigger immunity, systems can incorporate additional circuitry to ignore substantially simultaneous signals from both of the sensor channels. In general these systems do not make full use of the additional data which is available from two channel sensors.

3.1 PATTERN RECOGNITION SIGNAL PROCESSING

The additional information provided by a two-channel sensor can effectively be used by employing simple pattern recognition techniques. A block diagram of the intruder alarm unit is shown in Fig.4.

The system consists of three main sections:

a. Front end circuit.

Two stages of amplification and filtering which are duplicated to provide independent signal paths for each channel of the sensor.

b. Signal processing.

Output signals from the comparators are processed by a method known as Pattern Recognition.

c. Alarm unit.

An alarm condition raised by the signal processing section is used to drive a warning light and a relay.

Our patented signal processing, by the method of Pattern Recognition relies on the generation of unique pulse sequences at the comparator outputs. The sequence information occurring within a predetermined period of time is used to distinguish between intruder and non-intruder type signatures. Movement within the unit's field of view will generate a pulse train containing unique patterns. To allow sufficient time for all of the data to be gathered and processed a delay has been incorporated which is triggered on the leading edge of the first pulse and has a duration of 5 seconds.

3.2 INTRUDER PATTERNS

With this system eight intruder patterns have been defined, each of which comprises three sections. During an intruder disturbance at least one of these patterns occurs. The number of complete patterns depends on the intruder's speed and the unit's optical system. Patterns corresponding to movement of an intruder are tabulated in Table 2. If the two channels are labelled 'A' and 'B' respectively the positive peaks are denoted by '+A' and '+B' and negative peaks are denoted by '−A' and '−B'. Examples of timing diagrams corresponding to typical intruder events are shown in Figs.5a and 5b.

Pattern number	First in sequence	Second in sequence	Third in sequence
1	+A	+A and +B	+A
2	+A	+A and +B	+B
3	+B	+B and +A	+A
4	+B	+B and +A	+B
5	−A	−A and −B	−A
6	−A	−A and −B	−B
7	−B	−B and −A	−A
8	−B	−B and −A	−B

Table 2

3.3 FALSE TRIGGER PATTERNS

a. Thermal patterns

Changes in ambient temperature result in either random or no pattern being generated. Usually thermal patterns are not capable of generating more than one section of an intruder type signature and are therefore incomplete. Examples of timing diagrams corresponding to air turbulence and ambient temperature change situations are shown in Figs.5c and 5d respectively.

b. Radio Frequency interference (Rfi)

When subjected to 900 MHz radiated interference (6 mW into 50 Ω at a distance of 15 cm) random signal outputs are produced. Again these comparator transitions are only capable of triggering the first in sequence of the intruder signature and do not therefore initiate an alarm condition. An example of this behaviour is shown in the timing diagrams shown in Fig.5e.

4. CIRCUIT REALISATION

A block diagram of our Pattern Recognition signal processing circuit is shown in Fig.6. The blocks describe the major sections of the circuit in relation to the following functions:

a. THE DETECTION OF INTRUDER PATTERNS FOR BOTH CHANNELS

When the first in sequence of an intruder pattern is detected:

(i) a SET-RESET (S-R) type flip-flop remembers that event
(ii) the next block to look for the second in sequence is enabled

When the second in sequence of an intruder pattern is detected:

(i) an S-R type flip-flop remembers that event
(ii) the next block to look for the third in sequence is enabled

When the third in sequence of an intruder pattern is detected: an 'intruder sequence' memory is SET.

b. END OF SEQUENCE DETECTION

When all of the comparator outputs go LOW:

(i) an end of sequence has been detected
(ii) the first and second in sequence flip-flops are RESET.

c. TIMING PERIOD

When the first comparator in response to a disturbance goes HIGH: the transition is detected and the timer is triggered. Following the detection of such a disturbance, the flip-flops will be RESET when all four comparator outputs are LOW.

During the 5 second time delay:

(i) the timer's trigger is disabled to prevent retriggering
(ii) the alarm control unit output is disabled

When the 5 second time delay has expired:

(i) the alarm control unit output is enabled
(ii) the intruder sequence memory is RESET

d. ALARM CONTROL UNIT (ACU)

This monitors the outputs of both the intruder memory and system timer

(i) if an intruder sequence has been observed AND the time delay has expired then an alarm condition is raised

(ii) otherwise no alarm condition is raised

The numbers in Fig.6 refer to the waveforms at these points in the timing diagrams (see Figs.5a, 5b, 5c, 5d and 5e). Each diagram has a duration of 5 seconds.

4.1 CIRCUIT SCHEMATIC

Our Pattern Recognition signal processing circuit schematic is shown in Fig.7. This circuit consists of:

a. 43 logic gates
b. a 555 timer with associated timing components
c. an alarm RESET switch

At power up all of the flip-flop outputs are automatically set LOW, and the 'front end' circuit and detector time constants require the system to be RESET after an initial stabilisation period.

The descriptions of the logic gate functions are as follows:

a. Detection of the first in sequence of intruder type patterns as listed from 1 to 4 in Table 2 is achieved by using gates:

6a, 5a, 1a and 1b

— Gates 1a and 1b make up the S-R type flip-flop (f/f1)

b. Detection of the second in sequence of intruder patterns 1 to 4:

7a, 9a, 1c and 1d

— Gate 9a enables the second in sequence to be looked for following a f/f1 HIGH state transition, i.e. only after the detection of the first in sequence.

— Gates 1c and 1d make up the S-R type flip-flop (f/f2)

c. Detection of the third in sequence of intruder patterns 1 to 4:

4d, 6a and 12a

— Gate 12a enables the third in sequence to be looked for when the output of 9a switches to a LOW state.

d. Detection of the first in sequence of intruder type patterns as listed from 5 to 8 in Table 2 is achieved by gates:

6b, 5b, 2a and 2b

— Gates 2a and 2b make up the S-R type flip-flop (f/f3)

e. Detection of the second in sequence of intruder patterns 5 to 8:

7b, 9b, 2c and 2d

— Gate 9b enables the second in sequence to be looked for following a f/f3 HIGH state transition, ie only after the detection of the first in sequence.

— Gates 2c and 2d make up the S-R type flip-flop (f/f4)

f. Detection of the third in sequence of intruder patterns 5 to 8:

   4c, 6b and 12b

   – Gate 12b enables the third in sequence to be looked for when the output of 9b switches to a LOW state

g. The 'intruder sequence' memory, gates 3c and 3d is SET when any of the patterns 1 to 8 are seen as determined by gates 6d and 9c.

h. Timer triggering is achieved by use of gates:

   11a, 11b, 11c, 13a and IC14 (555 timer)

   – Gates 11a, 11b, and 11c look for the first leading edge.

   – Gate 13a is the trigger enable whereby the timer output, pin 3 is inverted via gate 8c and fed into the 'control' input of 13a disabling the trigger (pin 2) when the timer is on and enabling the trigger again when the time delay has expired.

i. End of sequence detection is determined via gates:

   11a, 11b, 11c, 8d, 12c, 12d, 11d, and 5d

   – Gates 11a, 11b, and 11c are employed here to look for no activity on the comparator output lines.

   – Gates 8d, 12c, 12d, 11d, and 5d look at the outputs of the S-R type flip-flops used to record the first in sequence of intruder patterns of both channels to see if they need to be RESET.

j. Alarm control unit:

   10a, 10b, 10c, 10d, 13b, 13c, 8c, 9d, 8a, 8b

   – Gates 8c and 9d gives an output from the ACU when the time delay has expired and the logical condition of an intruder exists.

   – Gates 8a and 8b holds an alarm condition if it appears at the outputs of the ACU. This can be RESET by a manually controlled push to break switch.

SUMMARY

The system described has been practically walk-tested for a wide range of intruder speeds at distances of up to 12 metres. Detection performance comparable with that of simple single-channel systems has been demonstrated. A prototype unit has been subjected to a number of potential false trigger sources including thermal disturbances and RF interference. The system provides considerably enhanced immunity to these phenomena which will result in a lower incidence of false triggers.

The logic circuit, which comprises a timer and a number of logic gates, may be implemented at a low cost with a single chip semi-custom integrated circuit.

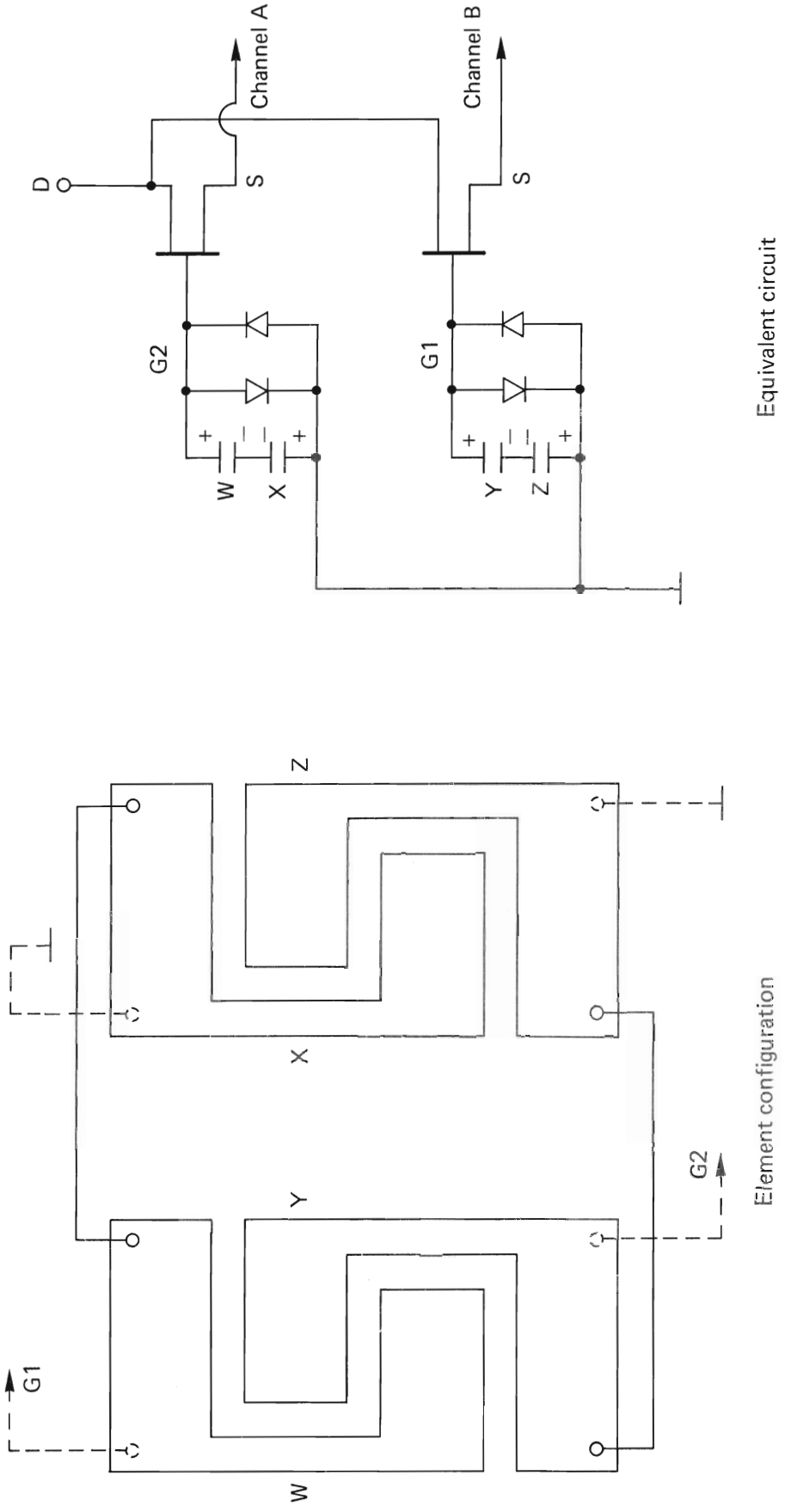


Fig.1 Element configuration of RPY222 two-channel sensor.

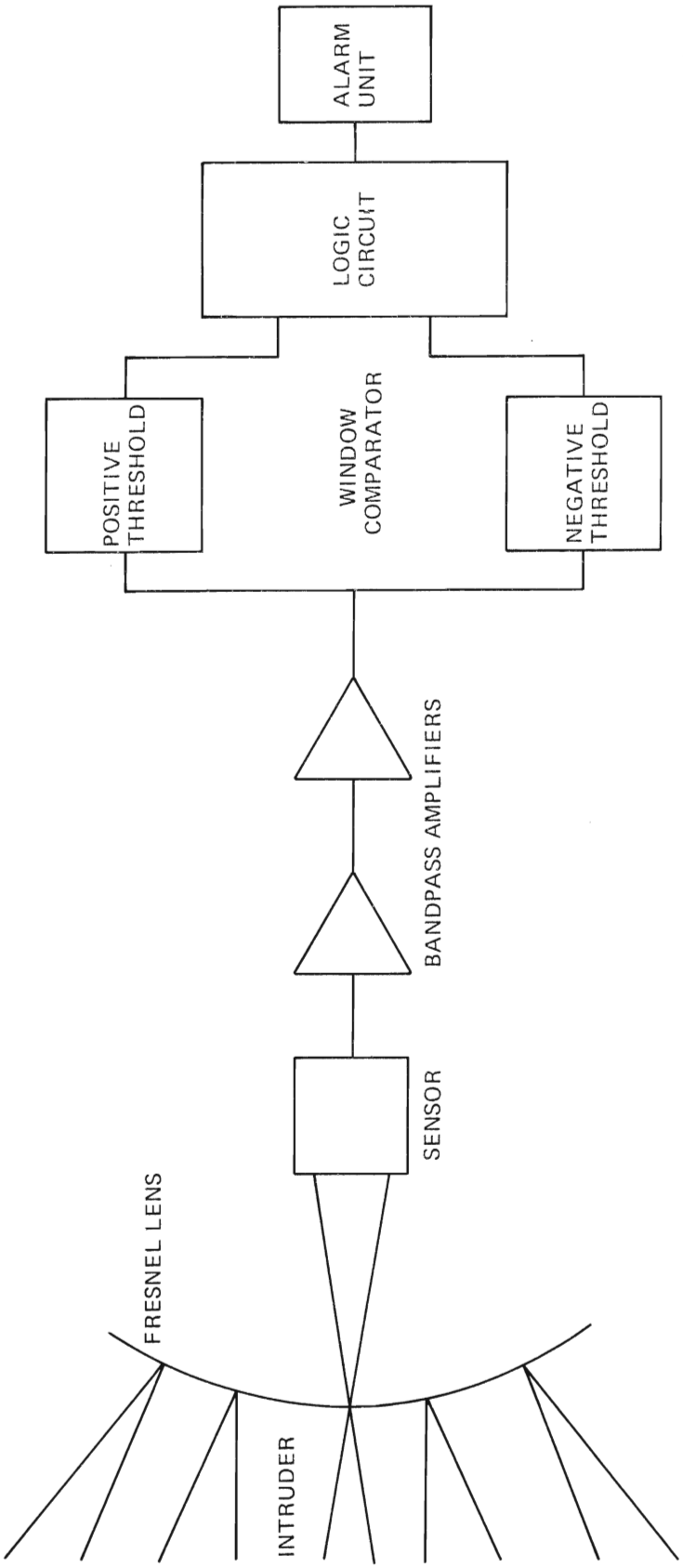


Fig.2 Passive infrared alarm system.

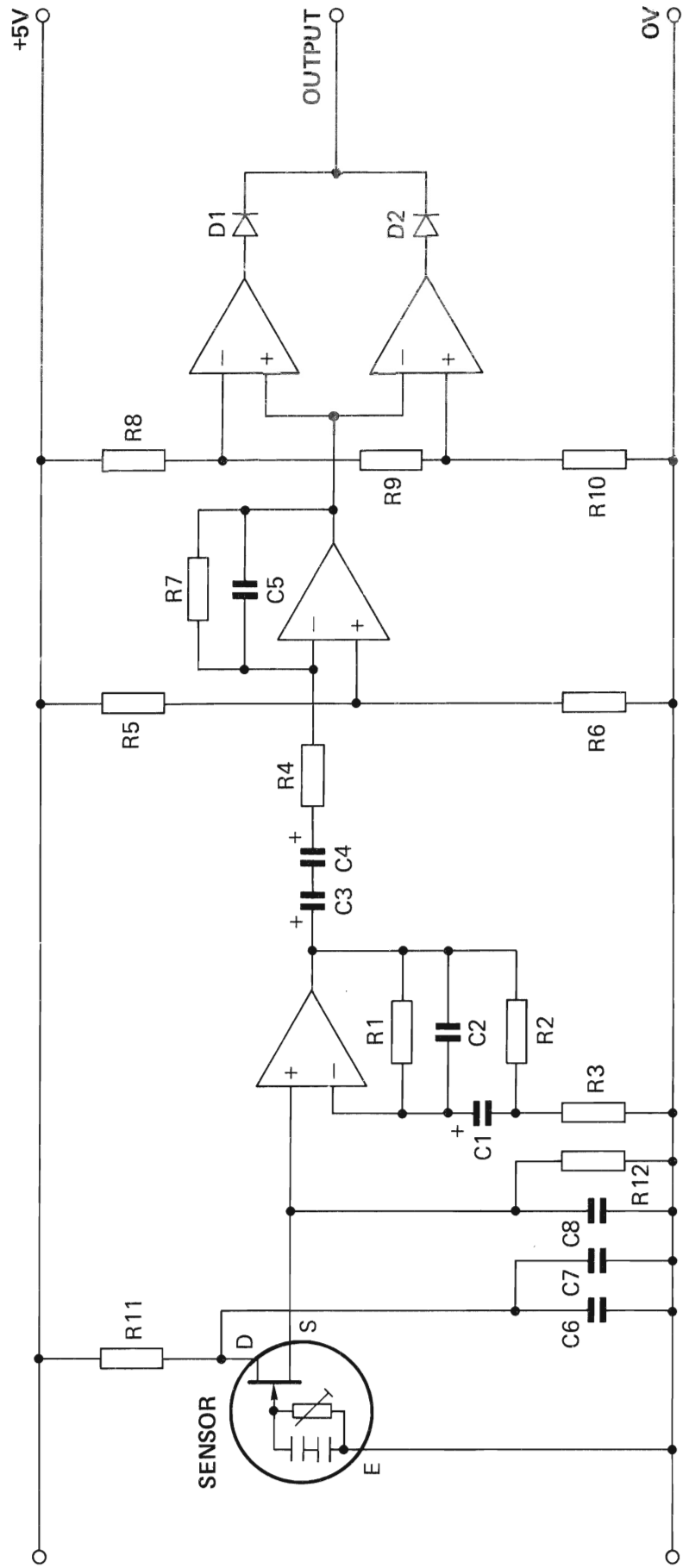


Fig.3 Front end signal processing circuitry for a conventional single-channel PIR system.

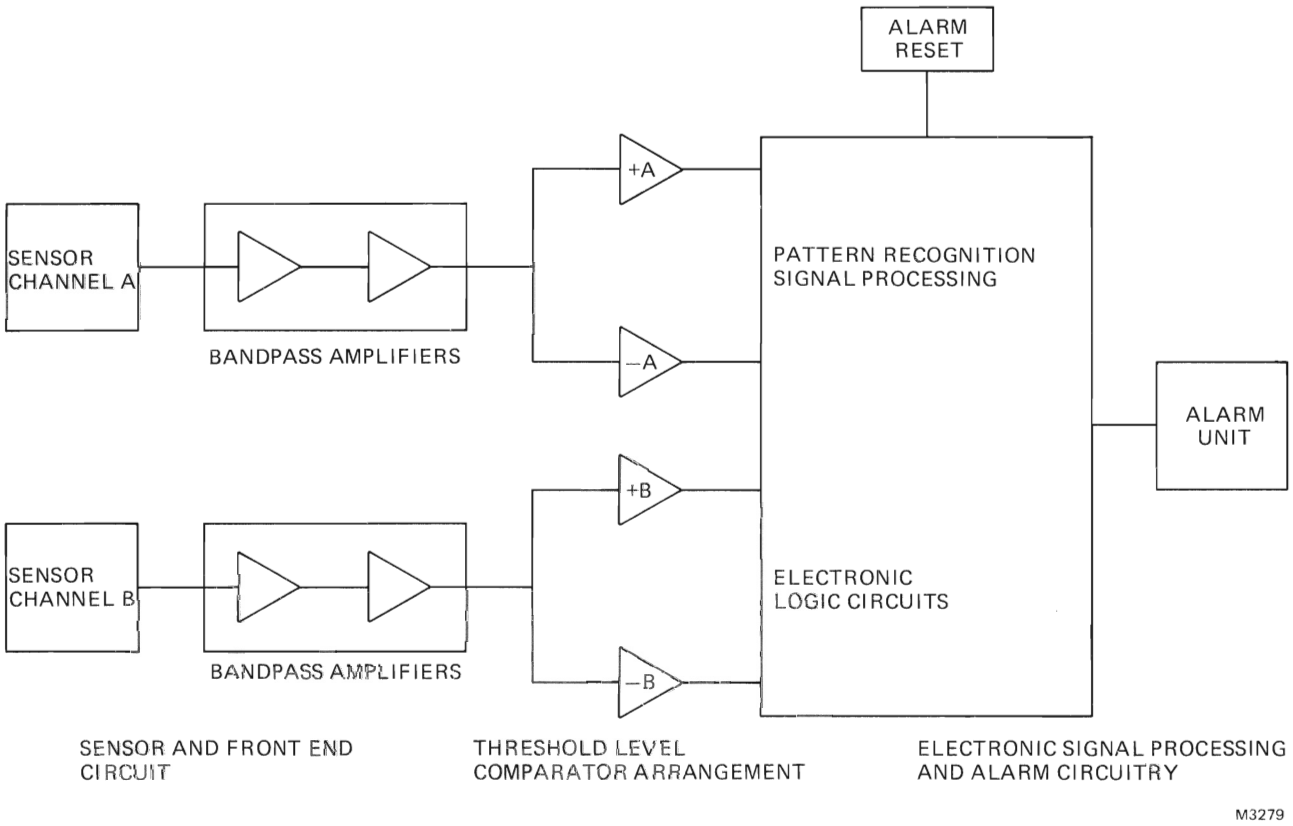


Fig.4 System block diagram.

15. Alarm
14. Time Delay
13. Not Connected
12. Intruder sequence detection
11. Third in sequence negative
10. Second in sequence negative
9. First in sequence negative
8. Third in sequence positive
7. Second in sequence positive
6. First in sequence positive
5. Timer trigger
4. End of sequence RESET
3. −B
2. +B
1. −A
0. +A

Fig.5 Key to timing diagrams in Figs.5a, b, c, d and e.

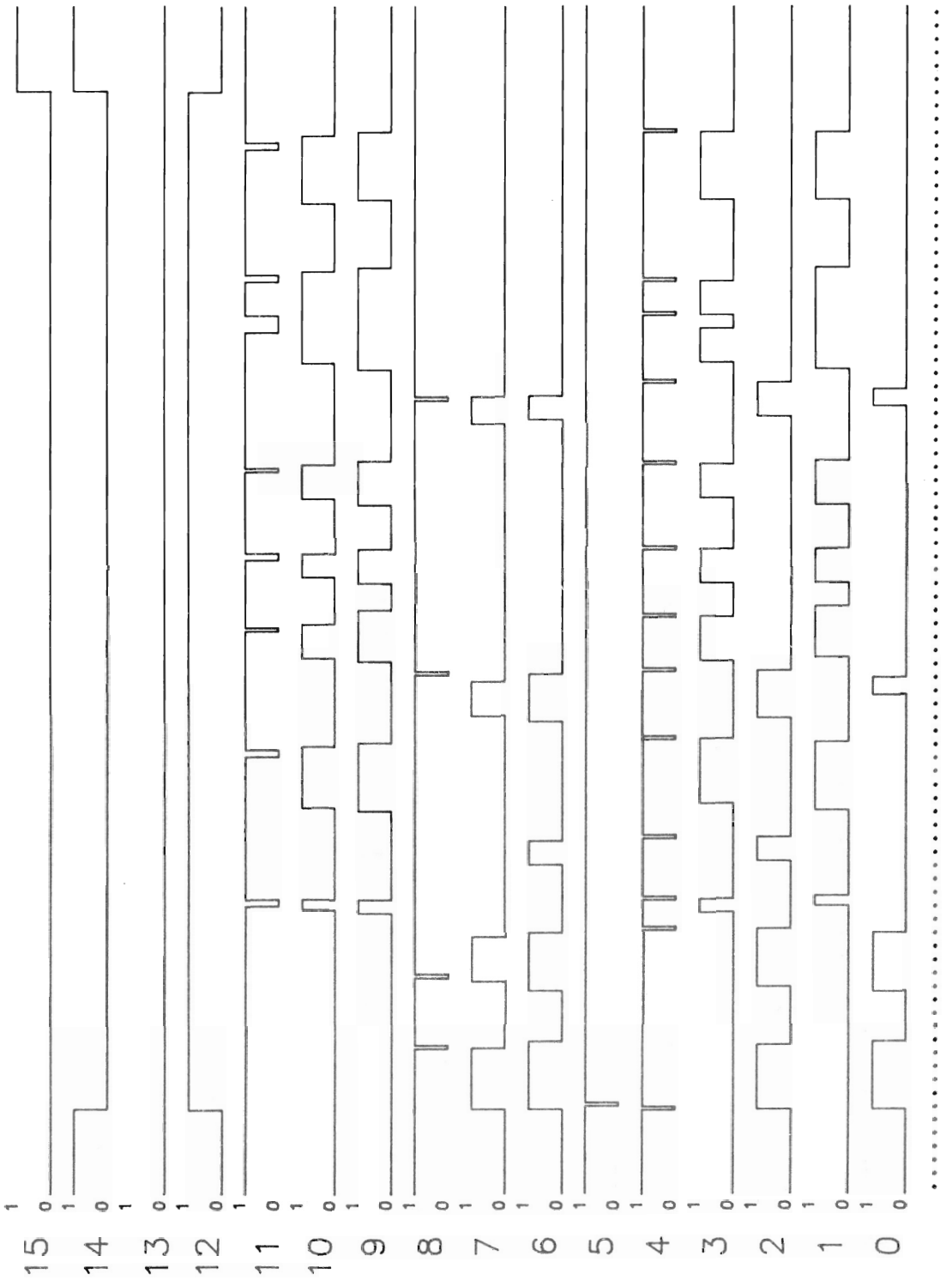


Fig.5a Intruder walking from left to right w.r.t. the detector.

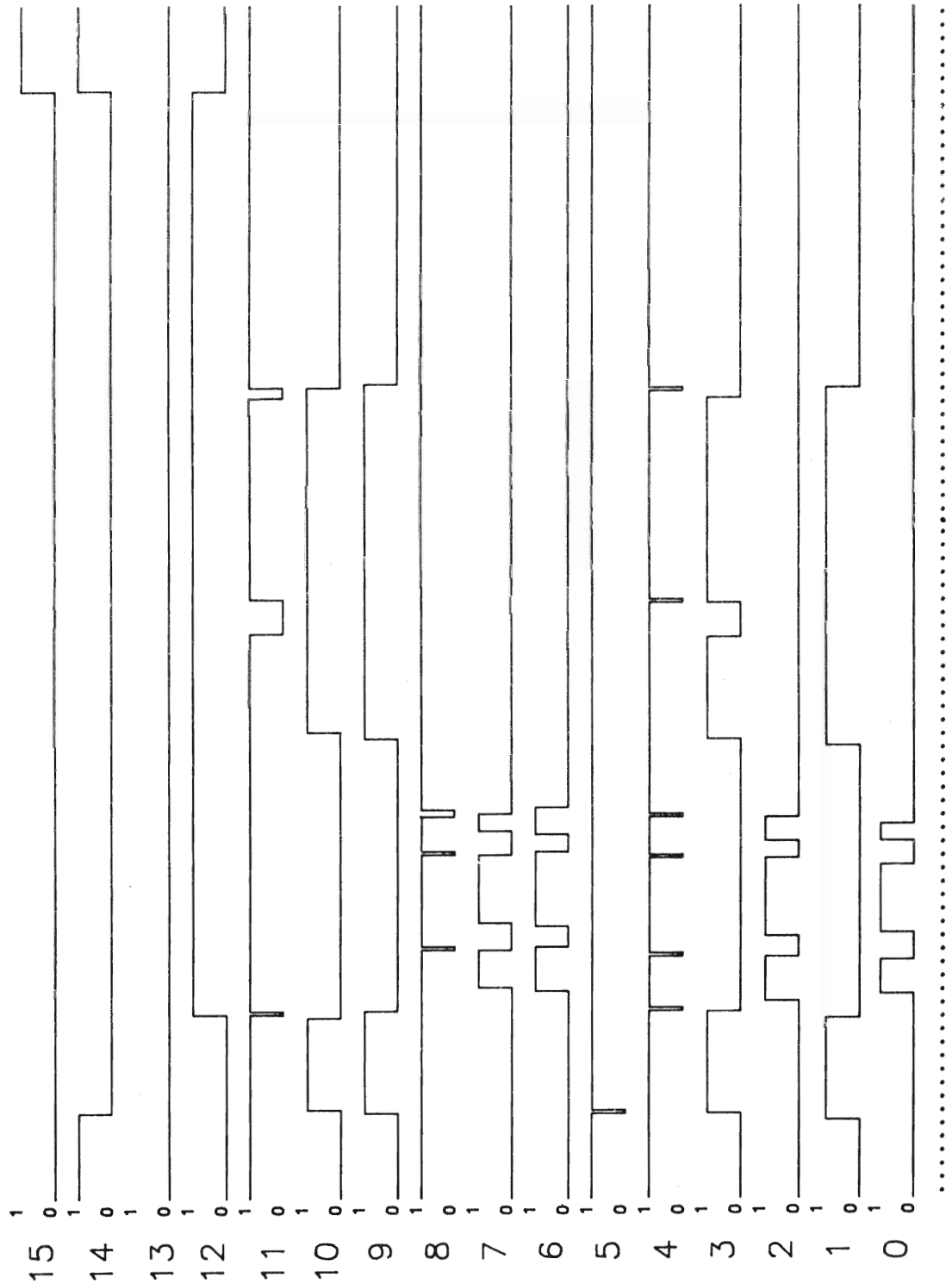


Fig.5b Intruder walking from right to left w.r.t. the detector.

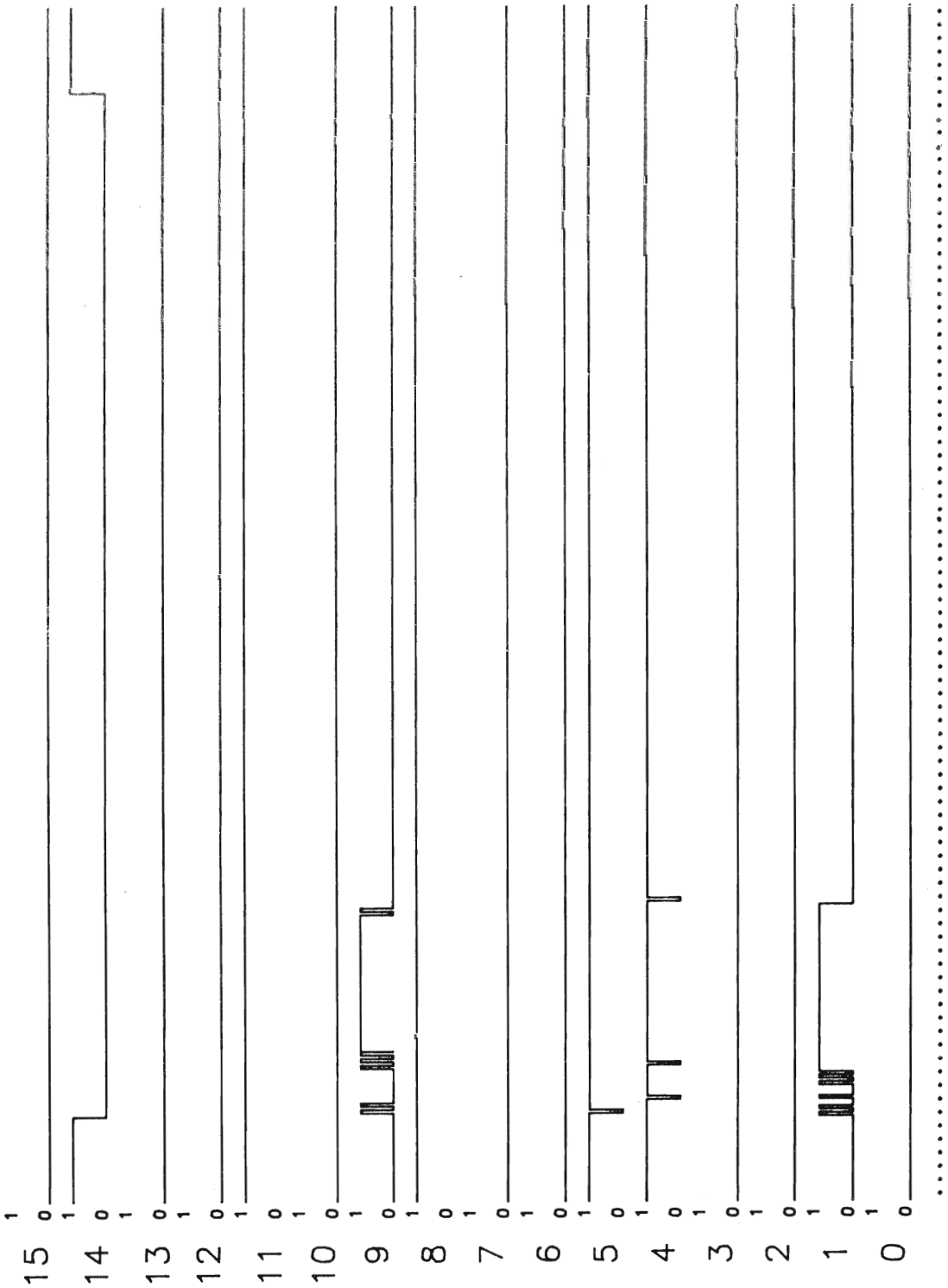


Fig.5c Response to a draught across the field of view.

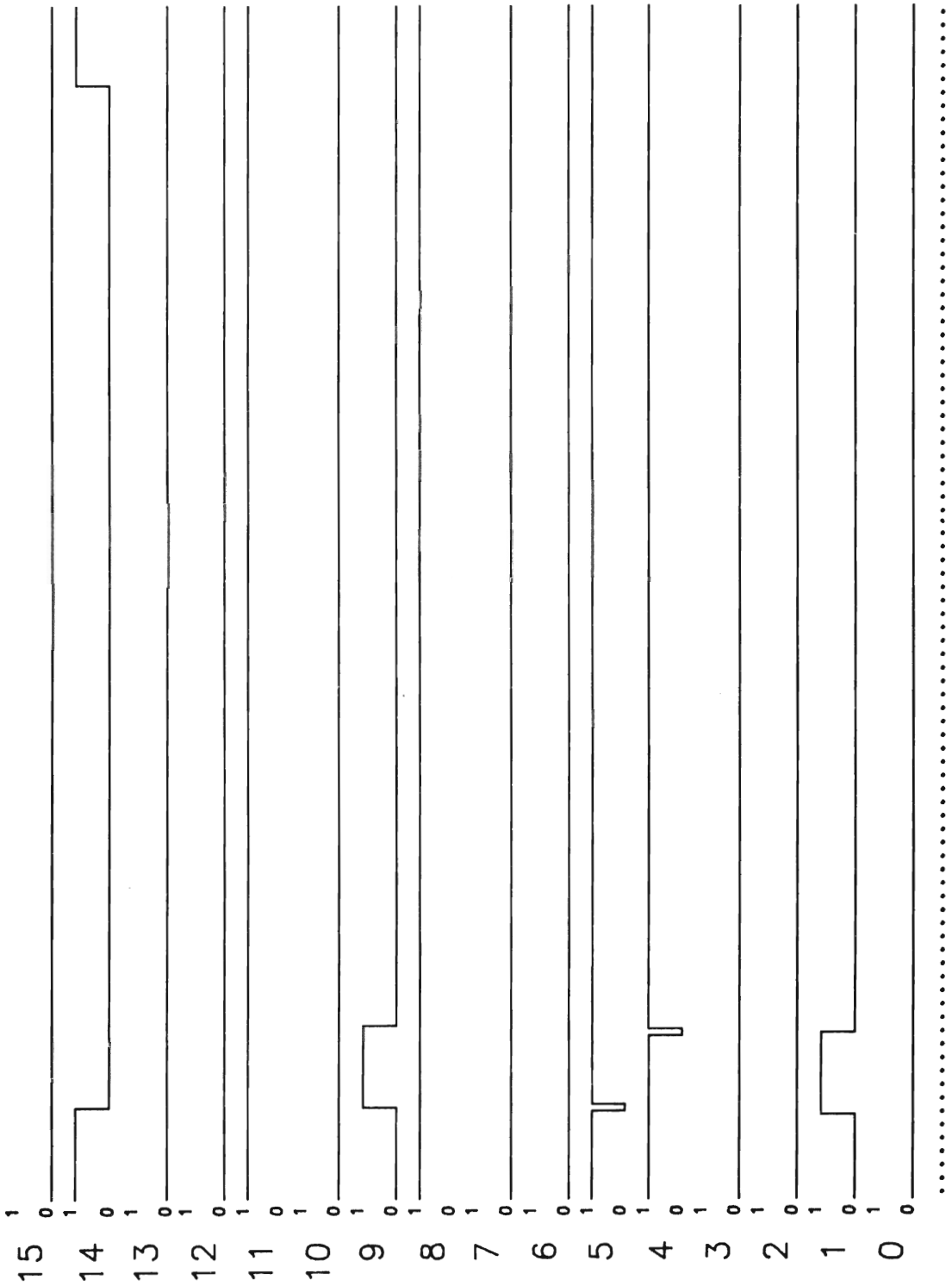


Fig.5d Response to a change in ambient temperature.

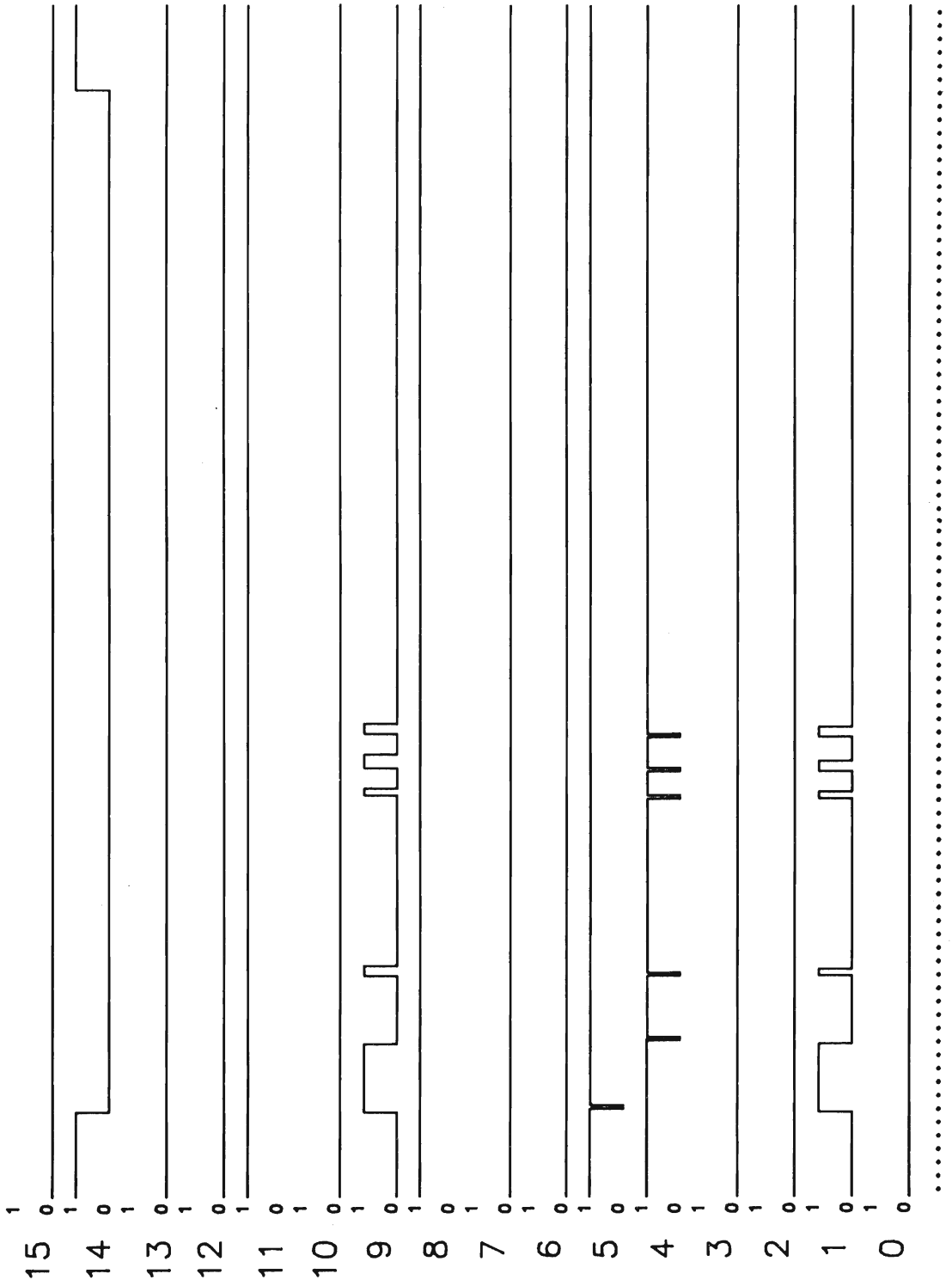


Fig.5e Response to an RF signal switching on and off.

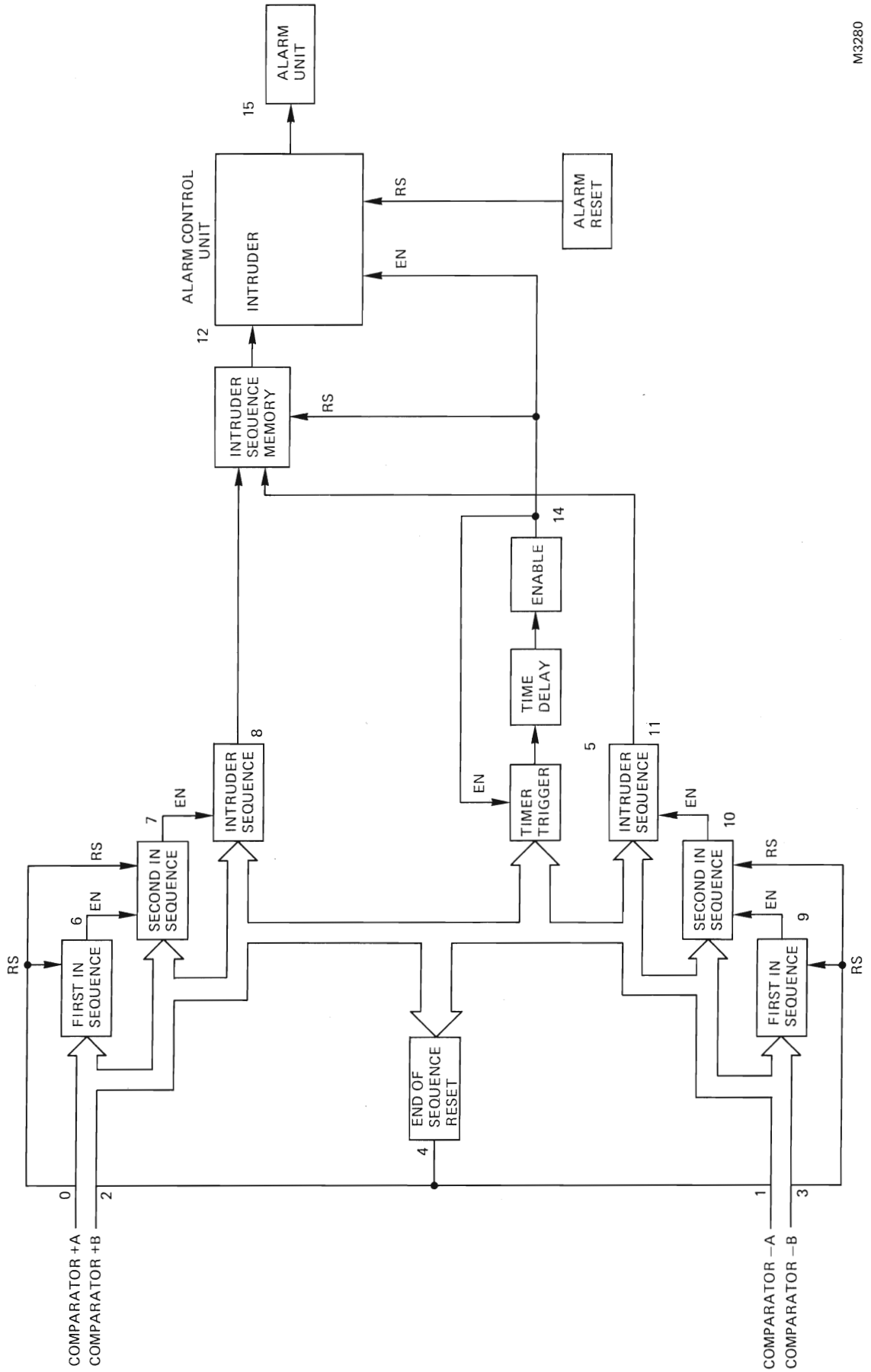


Fig.6 Block diagram of the Philips Components pattern recognition signal processing.

PHILIPS

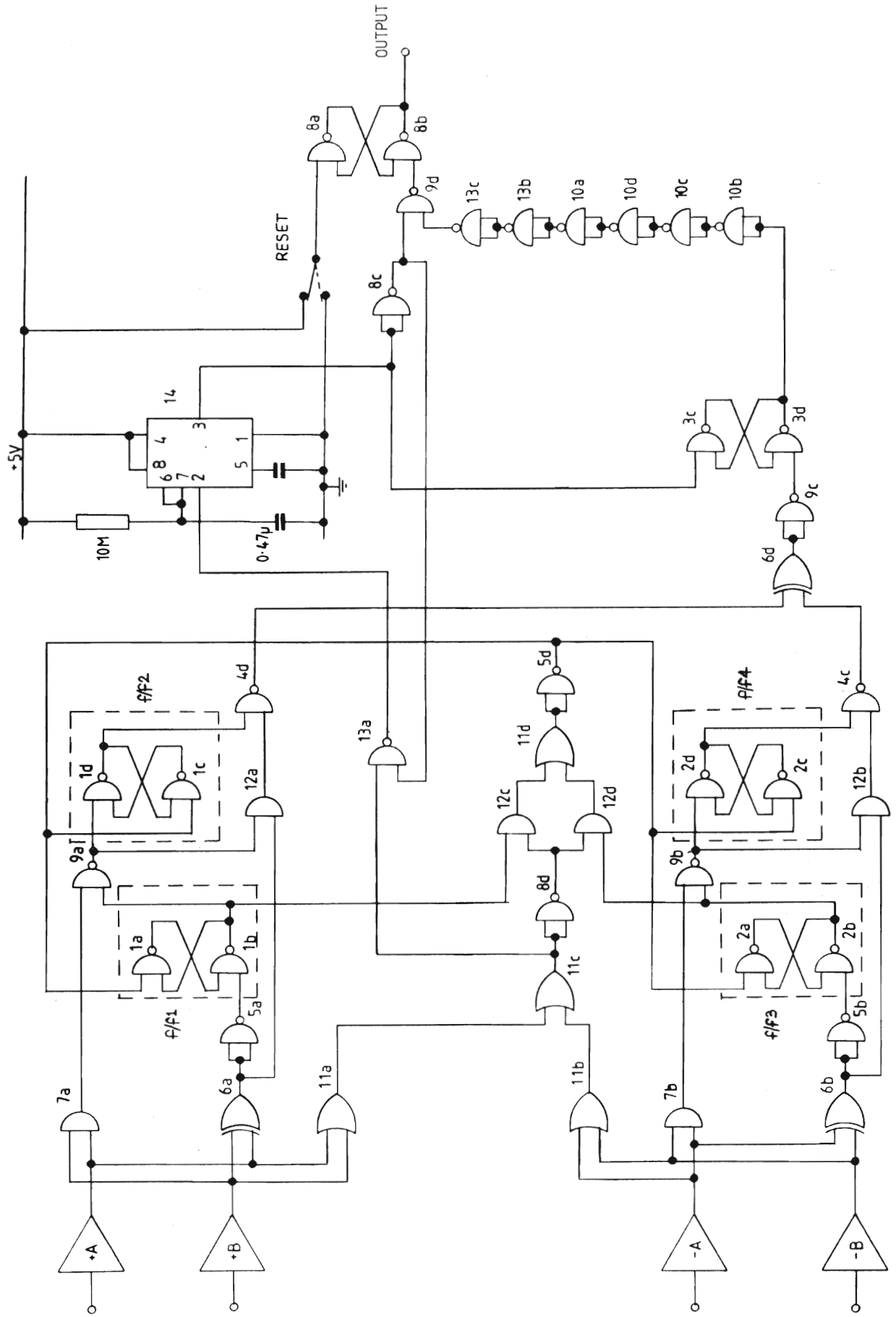


Fig.7 Circuit schematic of the Philips Components pattern recognition signal process.

Supersedes April 1988 data

TWO-CHANNEL PYROELECTRIC INFRARED SENSOR

Special features:	Two channels in one encapsulation to enable intelligent signal processing.
Application:	For use in passive IR intruder alarms.
Element configuration:	Two series-connected interdigitated pairs.
Electrical:	An impedance converting amplifier per channel, each having separate source connections.
Window:	Daylight filtered silicon.

QUICK REFERENCE DATA

Measured in source follower mode with 100 kΩ load resistor.

	min.	typ.	max.	
Spectral response	6.5 ± 0.5	–	>14	μm
Noise, peak-to-peak (bandwidth 0.4 Hz to 5 Hz)	–	30	55	μV
Peak signal (500K, 1) with incident energy of 25 μWcm^{-2}	570	850	1450	μV
Element dimensions and configuration		see page 2		
Operating voltage	3	–	10	V
Optimum operating frequency range	0.1	–	20	Hz

This data must be read in conjunction with GENERAL SAFETY RECOMMENDATIONS – OPTOELECTRONIC DEVICES.

MECHANICAL DATA

SOT-49N.

See page 2 for outline, element configuration and field of view diagrams.

MECHANICAL DATA

Dimensions in mm

Fig.1 SOT-49N.

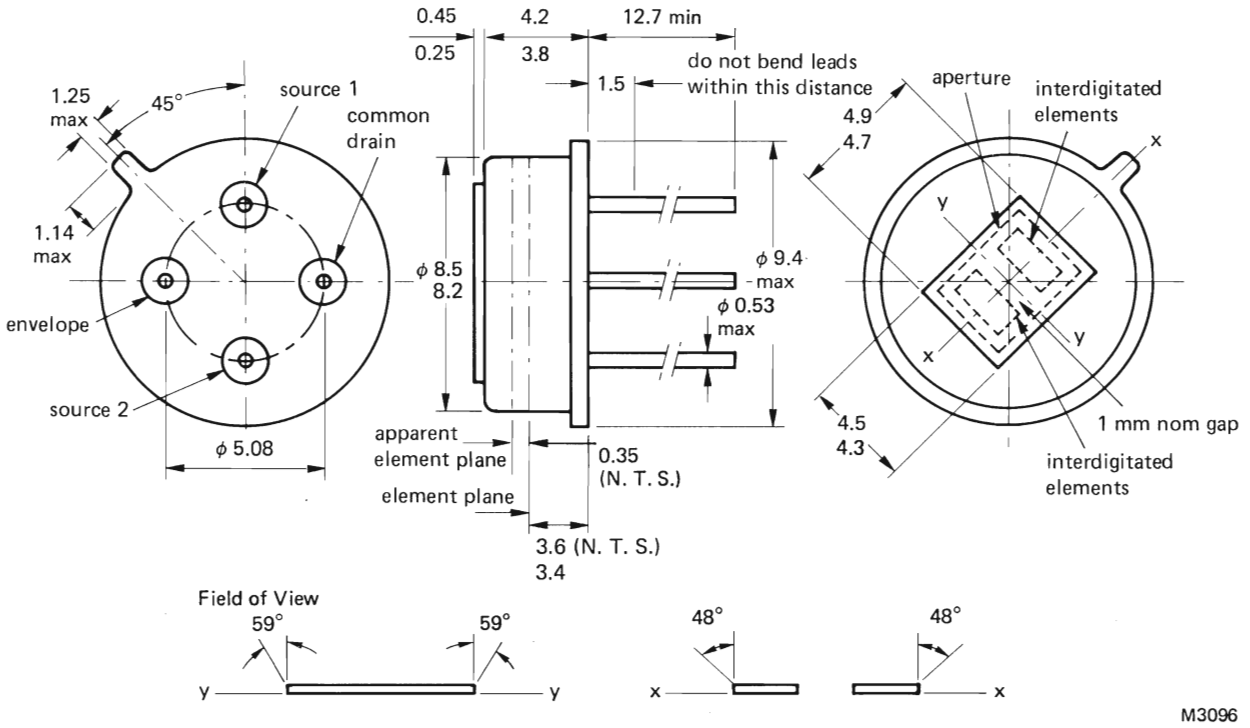
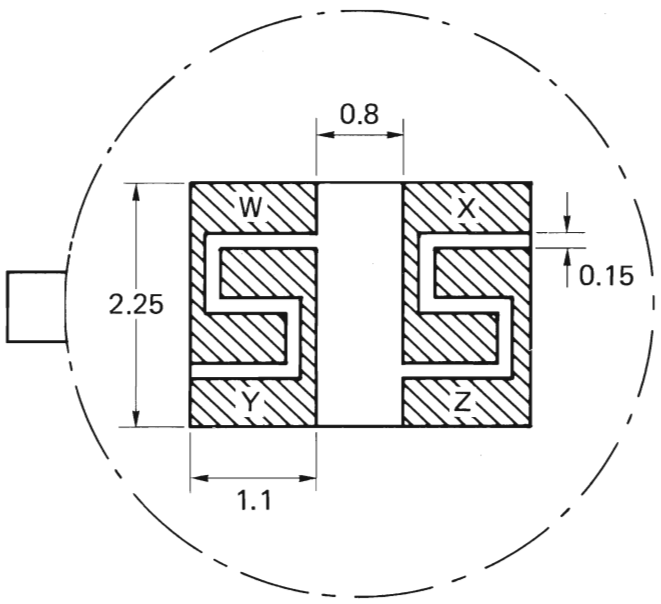


Fig.2 Element configuration.



PHILIPS

PRODUCT SAFETY

Modern high technology materials have been used in the manufacture of this device to ensure high performance. Some of these materials are toxic in certain circumstances. Mechanical or electrical damage is unlikely to give rise to any hazard, but toxic vapours may be generated if the device is heated to destruction. Disposal of large quantities should therefore be carried out in accordance with the latest local legislation.

SOLDERING

1. When making soldered connections to the leads, a thermal shunt should be used.
2. It is essential that any mains operated soldering iron used should be both screened and earthed. Failure to observe these precautions may lead to the introduction of line voltages and possible damage to the device. (see operating note 5)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134).

Supply voltage	max.	20	V
Temperature, operating range		−10 to +50	°C
Temperature, storage range		−30 to +70	°C
Lead soldering temperature, $\geqslant$6 mm from header, $t_{sld} \leqslant 3$ s		+350	°C

OPERATING NOTES

1. It is inadvisable to operate the sensor at mains related frequencies.
2. The case potential must not be allowed to become positive with respect to the other three terminals.
3. The sensor will operate outside the quoted range but may have a degraded performance.
4. To avoid the possibility of optical microphony, the sensor must be firmly mounted.
5. To avoid the possibility of electrostatic damage, precautions similar to those used with CMOS devices are necessary, namely:
   a) Earth wrist straps should be worn.
   b) Table tops or other working surfaces should be conductive and earthed.
   c) Anti-static clothing should be worn, (no wool, silk or synthetic fibres).
   d) No electrical testing should be carried out without specific, approved and written test procedures.
   e) To prevent the development of damaging transient voltages, devices should not be inserted into or removed from test fixtures with power applied.
6. An increase in temperature of elements W and Y will produce a positive going signal at the output. For elements X and Z, the corresponding output will be negative going.
7. Due to the high sensitivity of these sensors, care must be taken to ensure that the devices are allowed to become thermally stable before testing.

CHARACTERISTICS (at T_{amb} = 22 °C ± 3 °C and with recommended circuit)

Measured in source follower mode with 100 kΩ load resistor.

		min.	typ.	max.	
Spectral response		6.5 ± 0.5	–	>14	μm
Noise, peak-to-peak (bandwidth 0.4 Hz to 5 Hz) (note 1)		–	30	55	μV
Peak signal (500K, 1) with incident energy of 25 μWcm^{-2}		570	850	1450	μV
Dual element pair matching (note 2)		–	–	±20	%
Element dimensions and configuration			see page 2		
Field of view			see page 2		

F.E.T. Characteristics (at T_{amb} = 22 °C ± 3 °C)

Gate-source cut-off voltage I_D = 0.1 μA, V_{DS} = 6 V	$V_{(P)GS}$	−1.4	–	−0.5	V
Transfer conductance V_{GS} = 0, V_{DS} = 6 V, f = 1 kHz	g_{fso}	1.3	–	–	mAV^{-1}

Notes

1. Using low noise filter with 3 dB bandwidth (0.4 Hz to 5 Hz) and roll off at 12 dB per octave. Sensors tested for 1 minute under stable electrical and thermal conditions; see operating note 7 on page 3.
2. The matching of the elements is derived from $\frac{S_W - S_X}{\frac{1}{2}(S_W + S_X)} \times 100\%$, where S_W and S_X are the peak signal values of the respective elements. A similar calculation is applicable to elements Z and Y.

RECOMMENDED CIRCUIT

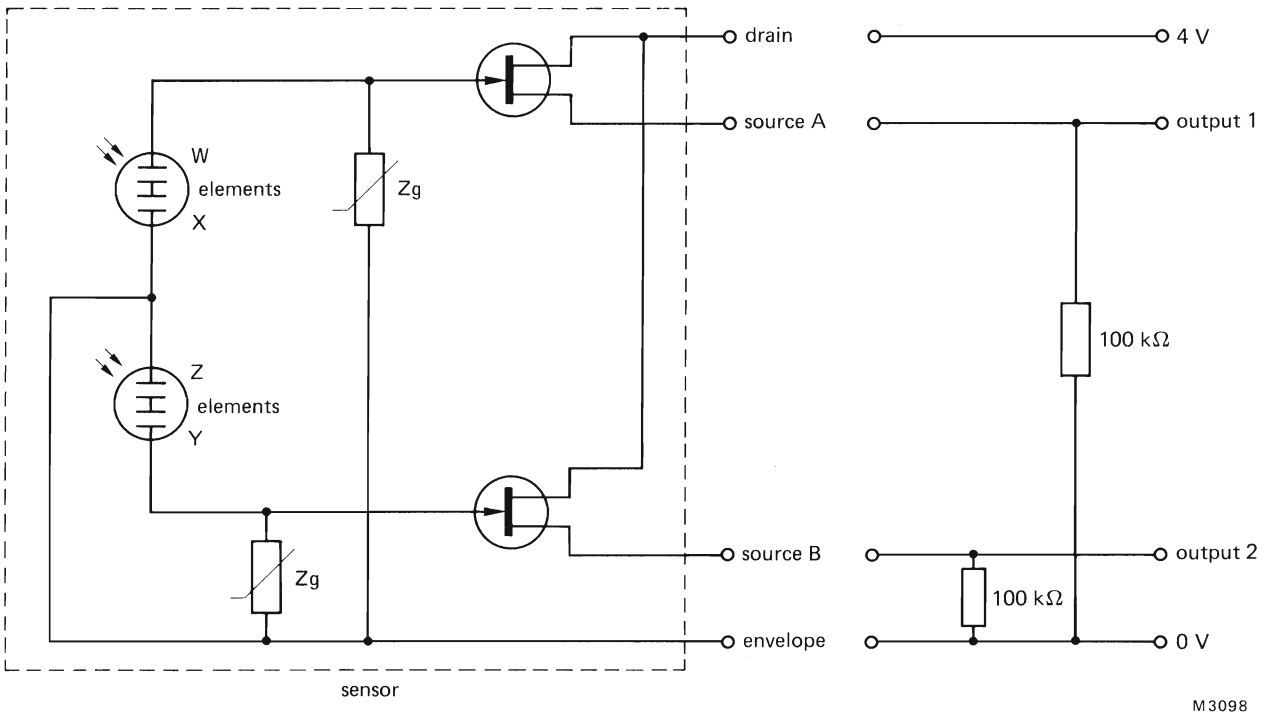


Fig.3.

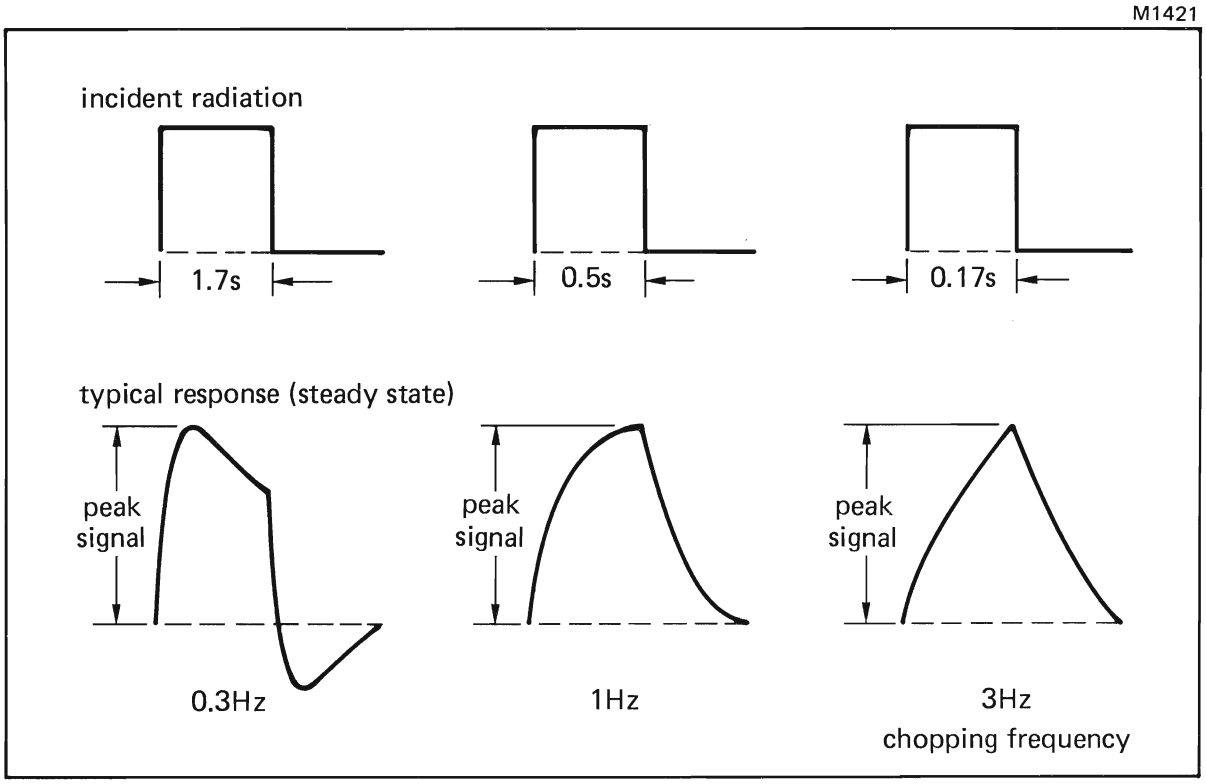


Fig.4 Typical response (steady state) for a given chopping frequency.

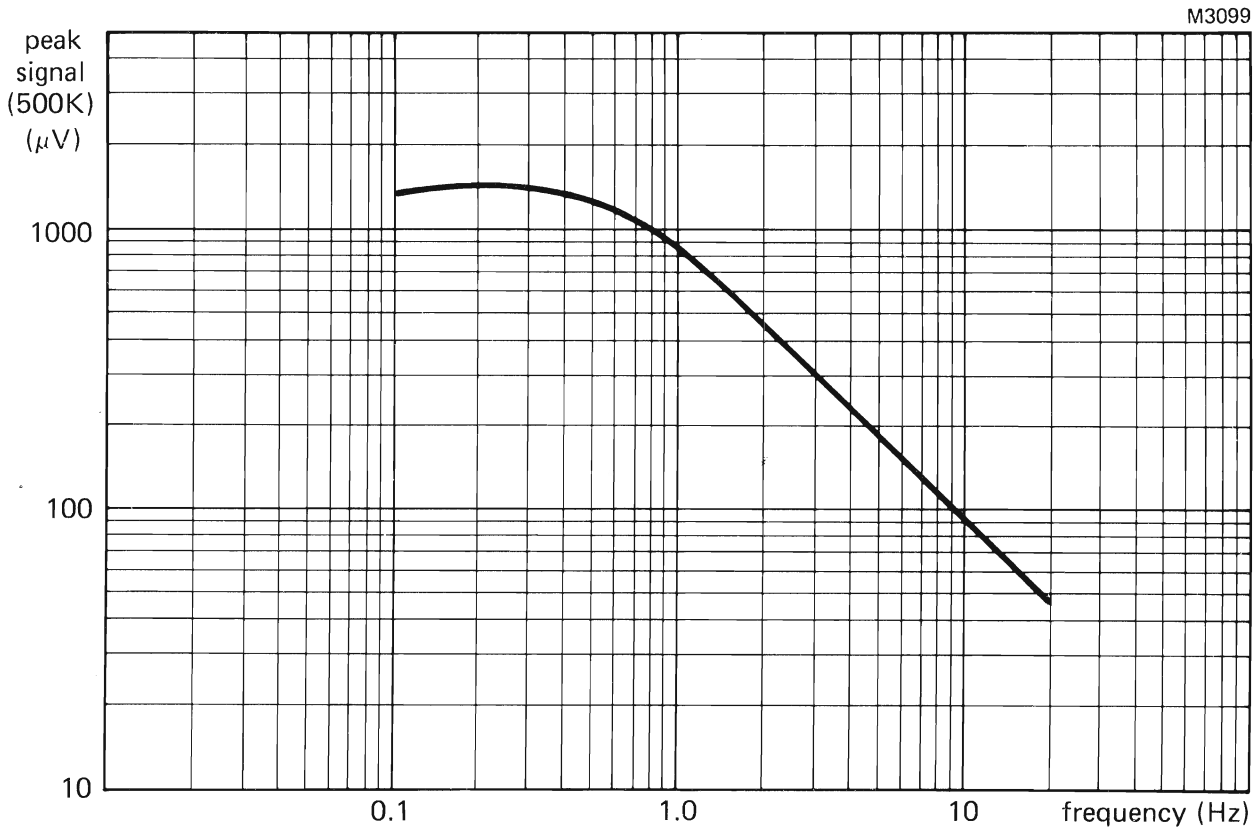


Fig.5 Typical peak signal as a function of frequency
(energy level 25 μWcm^{-2} at the element with the other element of the pair screened).

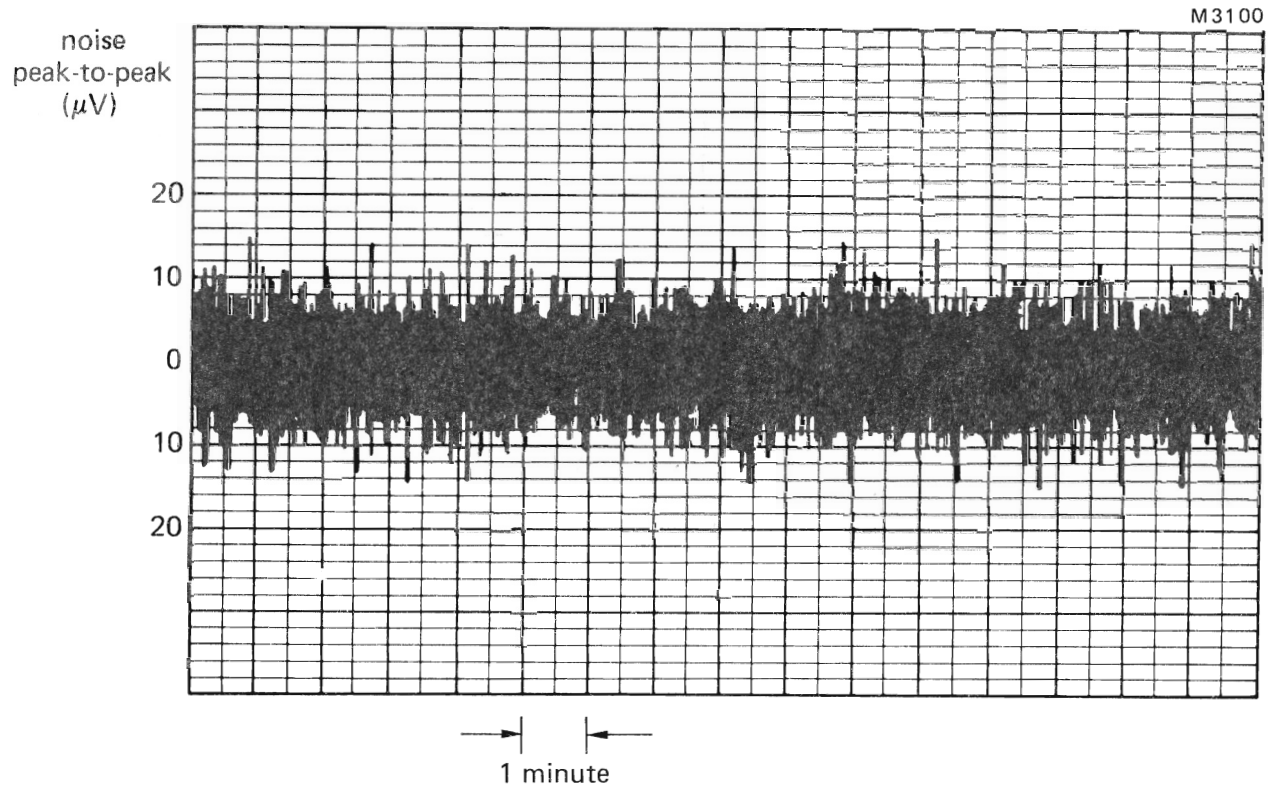


Fig. 6 Typical peak-to-peak noise as a function of time (filter bandwidth 0.4 Hz to 5 Hz).

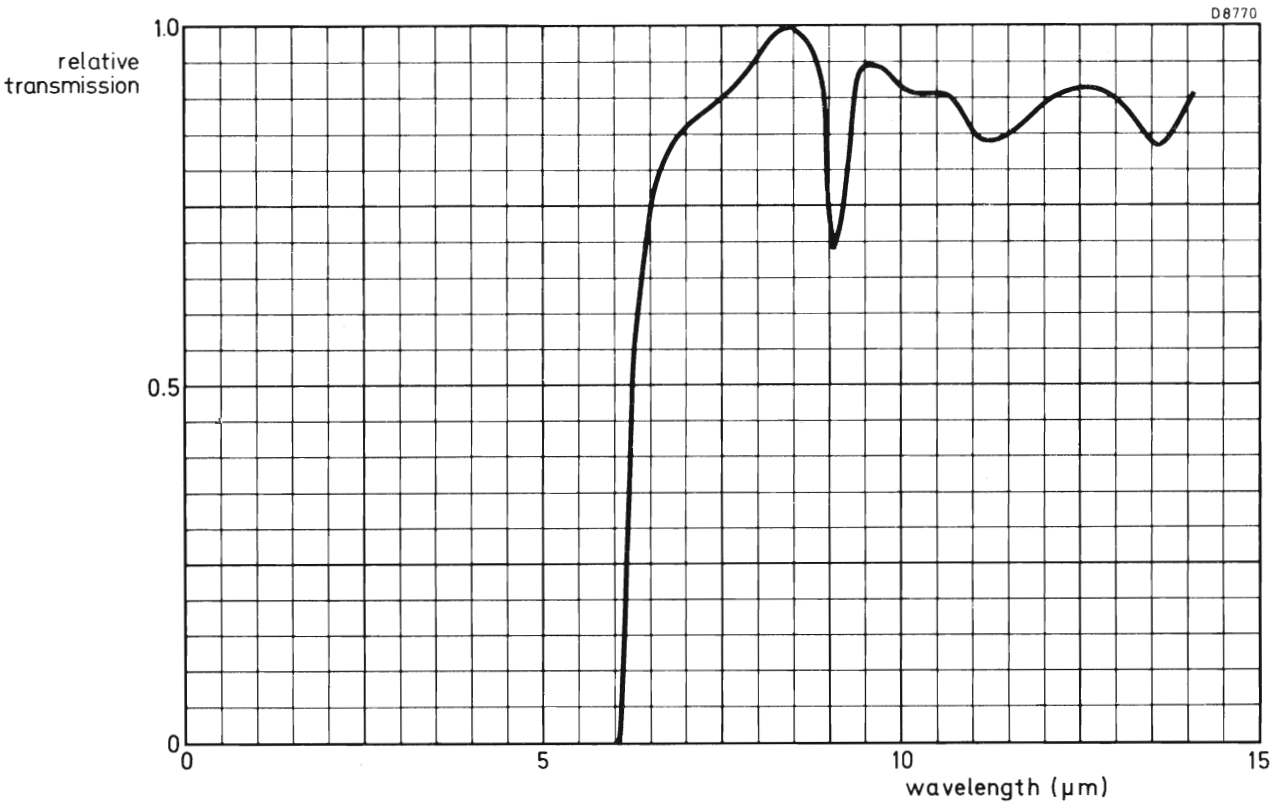


Fig.7 Typical normalized window transmission characteristic.

MECHANICAL AND ENVIRONMENTAL STANDARDS

As part of the Quality Assurance programme, the detectors will be assessed at regular intervals against the requirements of the following IEC standards. The frequency of testing and the limits and conditions for the pre- and post-test measurements are based on those stipulated for the CECC 50 000 series of approved transistors.

	Test		Severity	Duration	Note
IEC 68-2-4	D	Accelerated Damp Heat	+55 °C, 95% RH	6 cycles	1
68-2-20	Ta	Solderability	+235 °C, 1.5 mm from header	5 seconds	2
68-2-21	Ub	Lead Fatigue	4 cycles	—	2
68-2-1	Aa	Low Temperature Storage	−40 °C	2000 hours	2
68-2-2	Ba	High Temperature Storage	+70 °C	2000 hours	2
68-2-14	Nb	Change of Temperature	−40 °C to +70 °C	10 cycles	2
68-2-6	Fc (B4)	Vibration, swept frequency	125 Hz to 2 kHz 196 ms^{-2}	2 h in each orientation	2
68-2-27	Ea	Shock	14700 ms^{-2}	3 pulses 6 orientations	2
68-2-20	Tb	Resistance to Solder Heat	+350 °C, 6 mm from header	3 seconds	3

Notes

1. The detectors to be checked on a production batch release principle. This is equivalent to Group B.
2. The detectors to be checked at quarterly intervals. This is equivalent to Group C.
3. This is an annual check.

PATTERN RECOGNITION SIGNAL PROCESSING

1. INTRODUCTION

The performance of conventional PIR systems is ultimately limited by the amount of information that can be obtained from a standard dual element sensor. The RPY222 contains two independent sensors, the outputs of which can be processed separately to provide a degree of 'intelligence' and consequent reduction in false triggers (Ref.1).

The signal processing circuit for the RPY222 (Fig.1) basically consists of 43 standard logic gates and a timer IC. In order to eliminate the time consuming task of constructing this circuit, an evaluation board has been developed. This allows direct connection of the front end circuitry to a processing circuit providing all the necessary facilities for testing and evaluation.

The evaluation board consists of just two ICs and a few resistors and capacitors (Fig.2). One IC is the NE556 Dual Timer and the other is the Philips PLS155 Field-Programmable Logic Sequencer. The PLS155 allows all the logic functions of the signal processing circuit to be programmed onto the one 20 pin IC.

2. PLS155 PROGRAMMABLE LOGIC DEVICE (PLD)

Details on the architecture and features of this device can be found in the PLS155 data sheet, which is included in the Philips Components PLD data book (Ref.2).

Experience has shown that a circuit which has been designed using standard logic does not program efficiently onto a PLD. A better way to design programmable logic is to consider the system as a black box with a number of inputs and outputs. The system is then defined as a relationship between the inputs and outputs in the form of Boolean equations and state equations.

Defining a system in the form of a state diagram gives a visible representaion of the different states and the relationship between them. It can be seen from Fig.3 that there are two identical but completely separate state diagrams required to describe the overall system performance. One represents the state transition corresponding to the positive signals and the other to the negative signals.

Once all the necessary equations for the system have been defined, it is a fairly simple process, with the aid of the AMAZE software package, to program a device.

Firstly the pins are labelled and configured, according to the requirements of the system, using the pin-list editor (Fig.4). Then the Boolean equations are entered using the Boolean equation entry file (Fig.5). The flip-flops are also configured here, in this case all four are programmed to J-K Toggle mode.

The next stage is the entry of the state equations, which is performed using the state equation entry file (Fig.6). Information is entered into this file in a free format. A state transition language similar to Pascal is used, as can be seen in Fig.6.

Taking these three files, pin list file, Boolean entry file and state entry file, AMAZE can then "goto" assemble the information and produce a fuse map. The fuse map is represented in the form of a program table (Fig.7), which is the equivalent of a truth table.

Before down loading the fuse map to the programmer, the device can be checked for accurate operation using the AMAZE simulator. Any changes can then be made before the device is programmed, which can help to prevent unnecessary wastage of devices.

3. EXTERNAL CONNECTIONS (see Fig.8)

The only external connections are via connector 1

Pin 1	:	V_{CC} (+5 V)	
Pin 6	:	GND (0 V)	
Pin 2	:	+A	Comparator outputs from front end circuitry (note i)
Pin 3	:	−A	
Pin 4	:	+B	
Pin 5	:	−B	

Notes:

i. It is essential that the high to low transition on the comparator outputs are bounce free. Pull down resistors on the comparator outputs may be required.

4. ON-BOARD JUMPERS

J1: This jumper connects either one of the two alarm outputs to the LED, D1.

a) 'Alarm' pin 7 on IC1 indicates that an intruder sequence has been detected.

or

b) 'AlarmT' pin 19 on IC1 indicates that an intruder sequence has been detected **and** the time delay has elapsed.

J2: This jumper allows the time delay to be selected. The two resistors connected are R4 and R5 which have values of 10 MΩ and 4.7 MΩ respectively. The 10 MΩ value gives a time delay of approx 5 seconds and the 4.7 MΩ gives a time delay of approx 2.5 seconds. Alternative time delays can be easily implemented by changing R4 or R5 for values which can be calculated from the following equation:

$T \approx 1.1\ RC$ seconds where R = R4 or R5 in Ω
and C = C3 in F
(C3 = 0.47 μF)

5. STATE BITS

PT1 has four pins which give access to the values of the 4 state bits SB0, SB1, SB2 and SB3. By referring to the state transfer information, Fig.6, it is possible to monitor the bits and confirm that the system is operating correctly. They provide a valuable tool when fault finding.

6. CLOCK FREQUENCY

There are two main factors which determine the optimum clock frequency.

i. From experimental results it has been found that an intruder sequence can contain pulses (one from each channel) that differ in time by a minimum of approximately 10 ms. In order that these two pulses appear to have occurred at different moments in time, the clock speed must not be greater than 10 ms to provide adequate resolution.

ii. It has also been found that noise spikes which produce simultaneous signals on both channels can, as a result of amplitude and phase differences in the front end circuitry, appear at the comparator outputs slightly delayed with respect to each other. To try and counteract this problem the clock is made as slow as possible to ensure that these pulses appear to be simultaneous.

Taking these two constraints dictates an optimum clock speed of approximately 5 ms.

7. PCB

The component and track layout for side 1 and side 2 of the PCB can be seen in Fig.8 and Fig.9 respectively.

8. COMPONENT LIST

Resistors

R1	10 kΩ
R2	10 kΩ
R3	2.2 kΩ
R4	10 MΩ
R5	4.7 MΩ
R6	330 Ω
R7	6.8 kΩ

Capacitors

C1	1 μF
C2	1 μF
C3	0.47 μF
C4	330 nF
C5	22 nF
C6	22 nF
C7	2.2 nF
C8	2.2 nF
C9	10 μF
C10	0.1 μF
C11	1 μF
C12	47 μF

Semiconductors

IC1	PLS155	PLD
IC2	NE556	Dual timer
D1	LED	Standard

9. REFERENCES AND PUBLICATIONS

1. "Passive Infrared (PIR) Intruder Alarms", Philips Technical Publication, TP213, July 1986.
2. "Semi-custom Programmable Logic Devices (PLD)", Philips Data Handbook, IC13.
3. "Introduction to RPY222 sensor", see pages 1 to 17 of this publication.

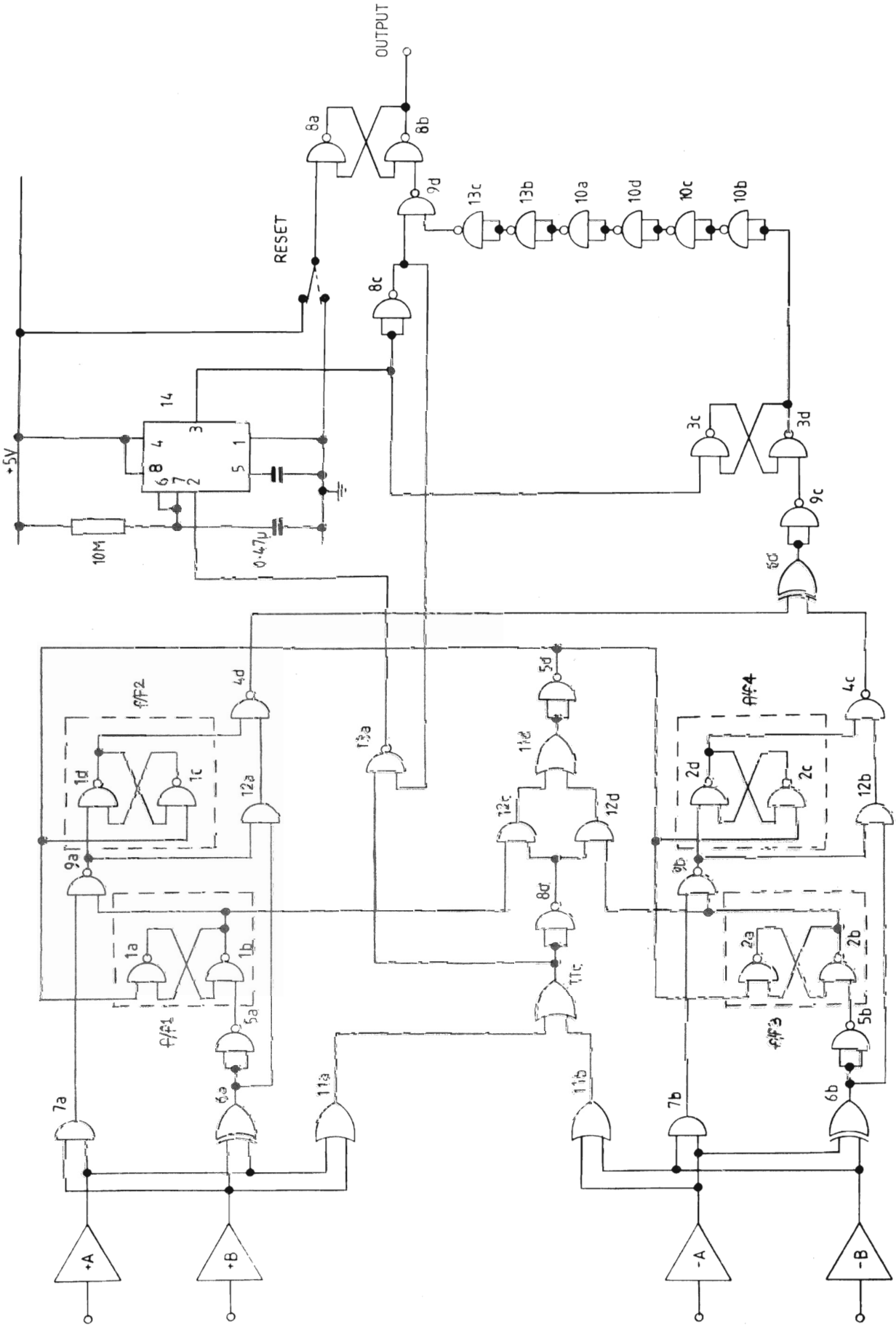


Fig.1 Signal processing circuit using standard logic.

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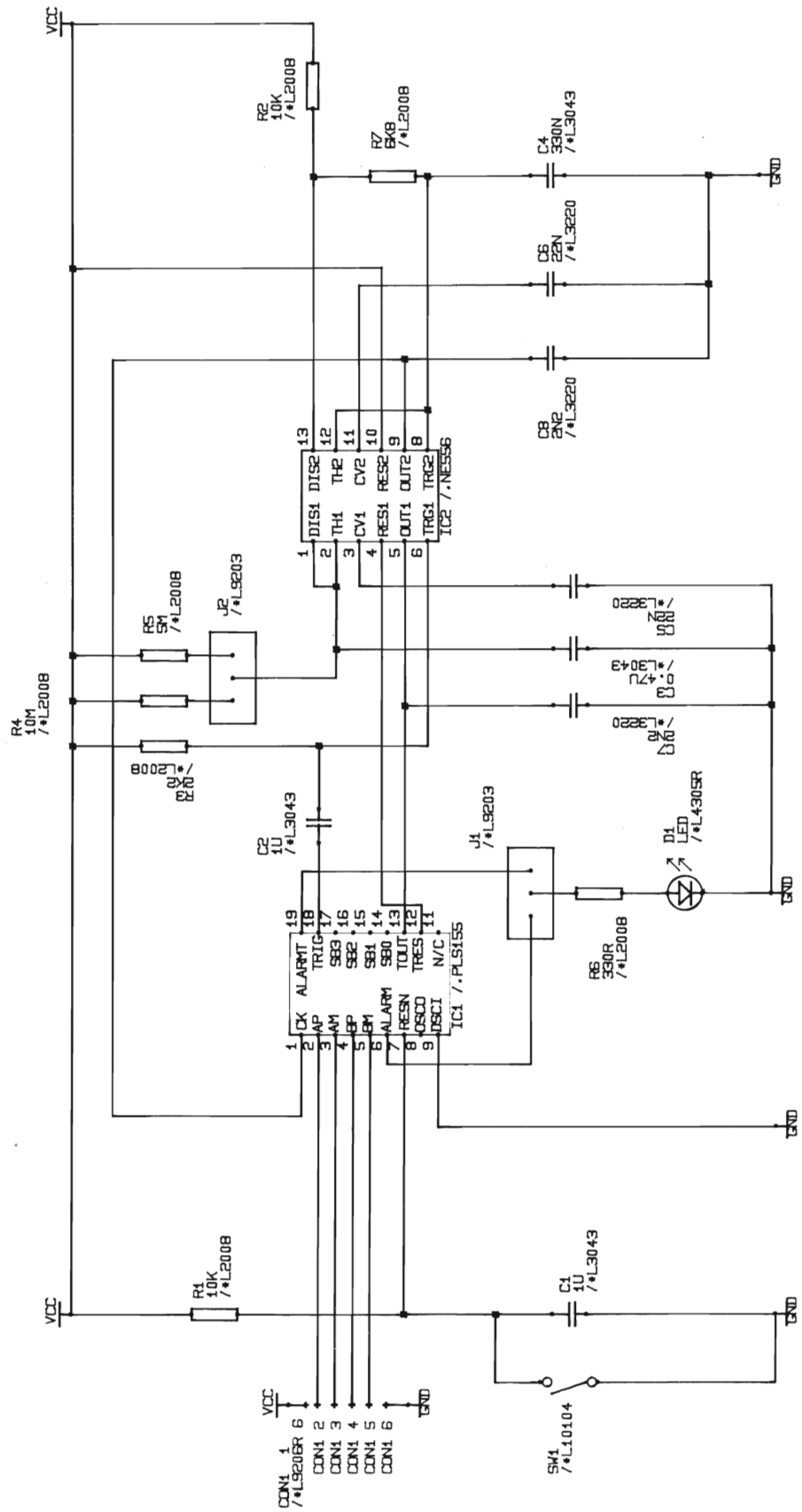

Fig.2 Signal processing circuit using a PLS155.

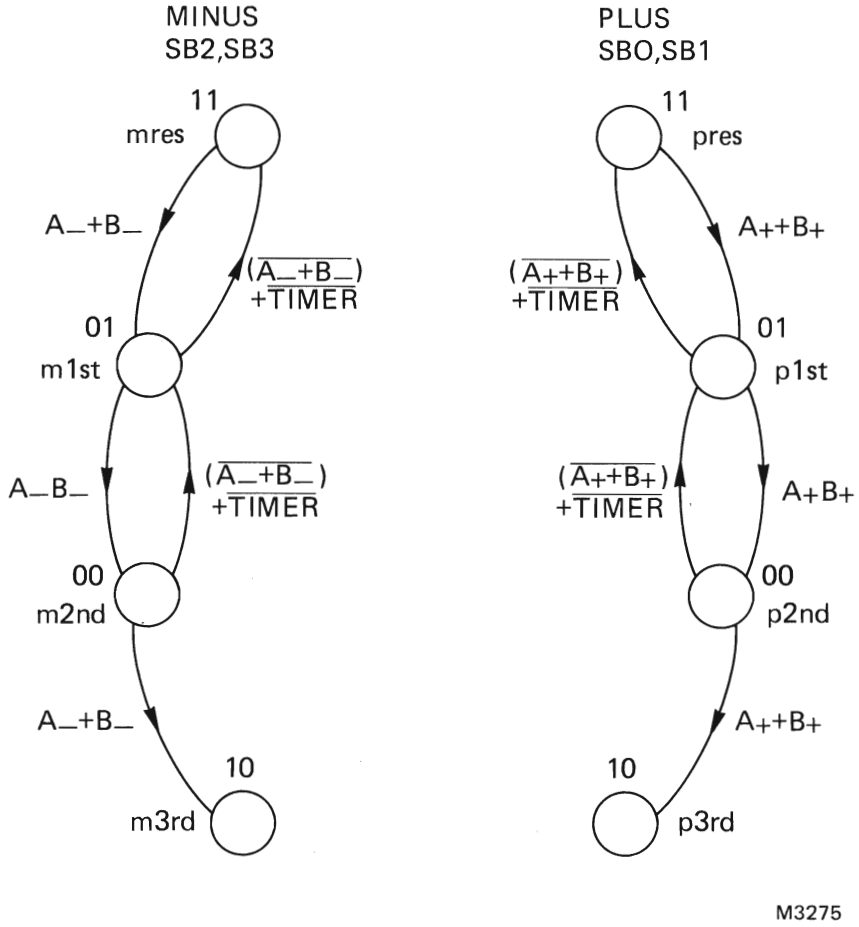

Fig.3 State diagram representation of system.

P I N L I S T

LABEL	**	FNC	**	PIN		PIN	**	FNC	**	LABEL
CLOCK	**	CK	**	1–I		I–20	**	+5V	**	VCC
AP	**	I	**	2–I		I–19	**	O	**	ALARMT
AM	**	I	**	3–I	P	I–18	**	/O	**	TRIGGER
BP	**	I	**	4–I	L	I–17	**	/O	**	SB3
BM	**	I	**	5–I	S	I–16	**	/O	**	SB2
ALARM	**	O	**	6–I	1	I–15	**	/O	**	SB1
RESETN	**	I	**	7–I	5	I–14	**	/O	**	SB0
OSCO	**	O	**	8–I	5	I–13	**	I	**	TIMEOUT
OSCI	**	/B	**	9–I		I–12	**	/O	**	TIMRES
GND	**	0V	**	10–I		I–11	**	/DE	**	N/C

Fig.4 AMAZE pin list file.

```
@DEVICE TYPE
PLS155
@DRAWING
@REVISION
@DATE
@SYMBOL
@COMPANY
@NAME
@DESCRIPTION
@COMMON PRODUCT TERM

res =sb0*sb1*sb2*sb3;

@COMPLEMENT ARRAY

/c =/(res);

@I/O DIRECTION

d3 =osco;

@FLIP FLOP CONTROL

fc =1;

@OUTPUT ENABLE
@REGISTER LOAD
@ASYNCHRONOUS PRESET/RESET
@FLIP FLOP MODE
@LOGIC EQUATION

"timer"

trigger=/(/c*resetn);
timres=/(res+alarmt+/resetn);

"alarm outputs"

alarm = (sb0*/sb1)+(sb2*/sb3);
alarmt=((sb0*/sb1)+(sb2*/sb3))*/timeout;
```

Fig.5 AMAZE Boolean Equation entry file.

```
@DEVICE SELECTION

alarm/pls155

@STATE VECTORS

 [sb0,sb1,sb2,sb3]

pres  = 11--b;
p1st  = 01--b;
p2nd  = 00--b;
p3rd  = 10--b;
pjmp  = -1--b;
mres  = --11b;
m1st  = --01b;
m2nd  = --00b;
m3rd  = --10b;
mjmp  = ---1b;
all   = ----b;
reset = 1111b;

@INPUT VECTORS
@OUTPUT VECTORS
@TRANSITIONS

"plus inputs"

while [pres]
   if [ap*/bp*resetn]            then [p1st]
   if [/ap*bp*resetn]            then [p1st]
while [p1st]
   if [/ap*/bp*resetn*timeout]   then [pres]
   if [ap*bp*resetn*timeout]     then [p2nd]
   if [/timeout*resetn]          then [pres]
while [p2nd]
   if [ap*/bp*resetn*timeout]    then [p3rd]
   if [/ap*bp*resetn*timeout]    then [p3rd]
   if [/ap*/bp*resetn*timeout]   then [pjmp]
   if [/timeout*resetn]          then [pjmp]

"minus inputs"

while [mres]
   if [am*/bm*resetn]            then [m1st]
   if [/am*bm*resetn]            then [m1st]
while [m1st]
   if [/am*/bm*resetn]           then [mres]
   if [am*bm*resetn]             then [m2nd]
   if [/timeout*resetn]          then [mres]
while [m2nd]
   if [am*/bm*resetn*timeout]    then [m3rd]
   if [/am*bm*resetn*timeout]    then [m3rd]
   if [/am*bm*resetn*timeout]    then [mjmp]
   if [/timeout*resetn]          then [mjmp]

"reset"

while [all]
   if [/resetn]                  then [reset]
```

Fig.6 AMAZE state equation entry file.

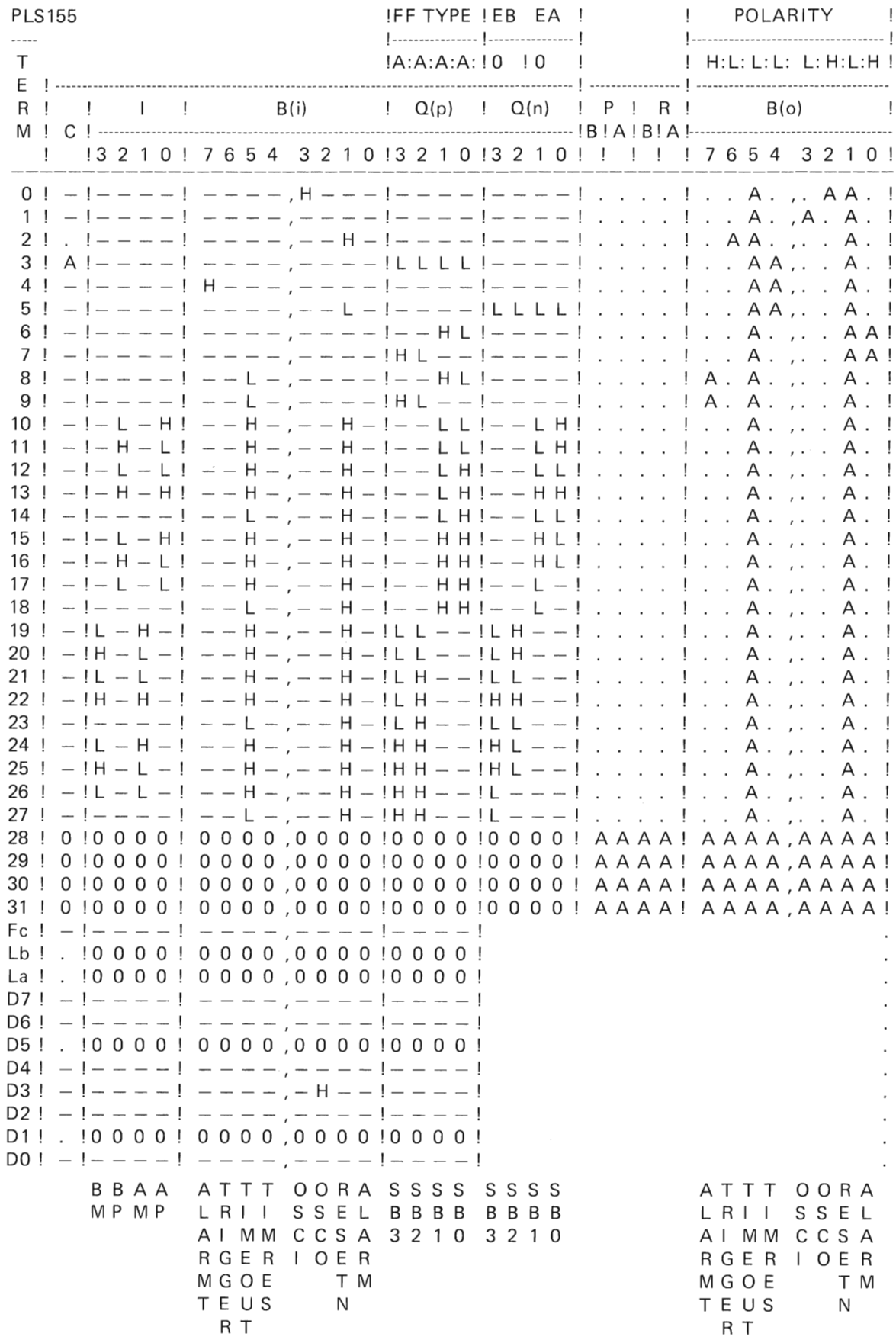

Fig.7 AMAZE fuse map.

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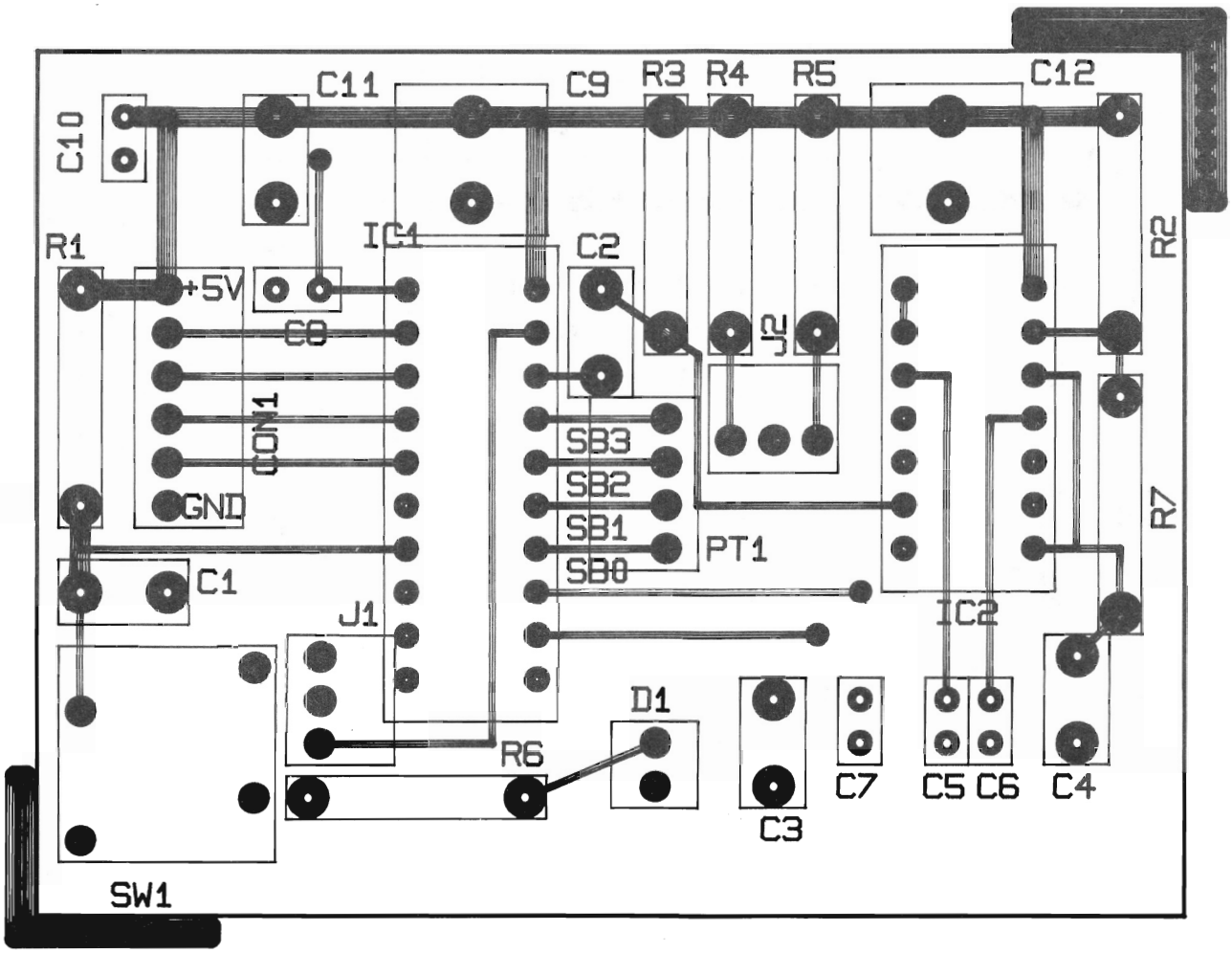

Fig.8 PCB layout (side 1).

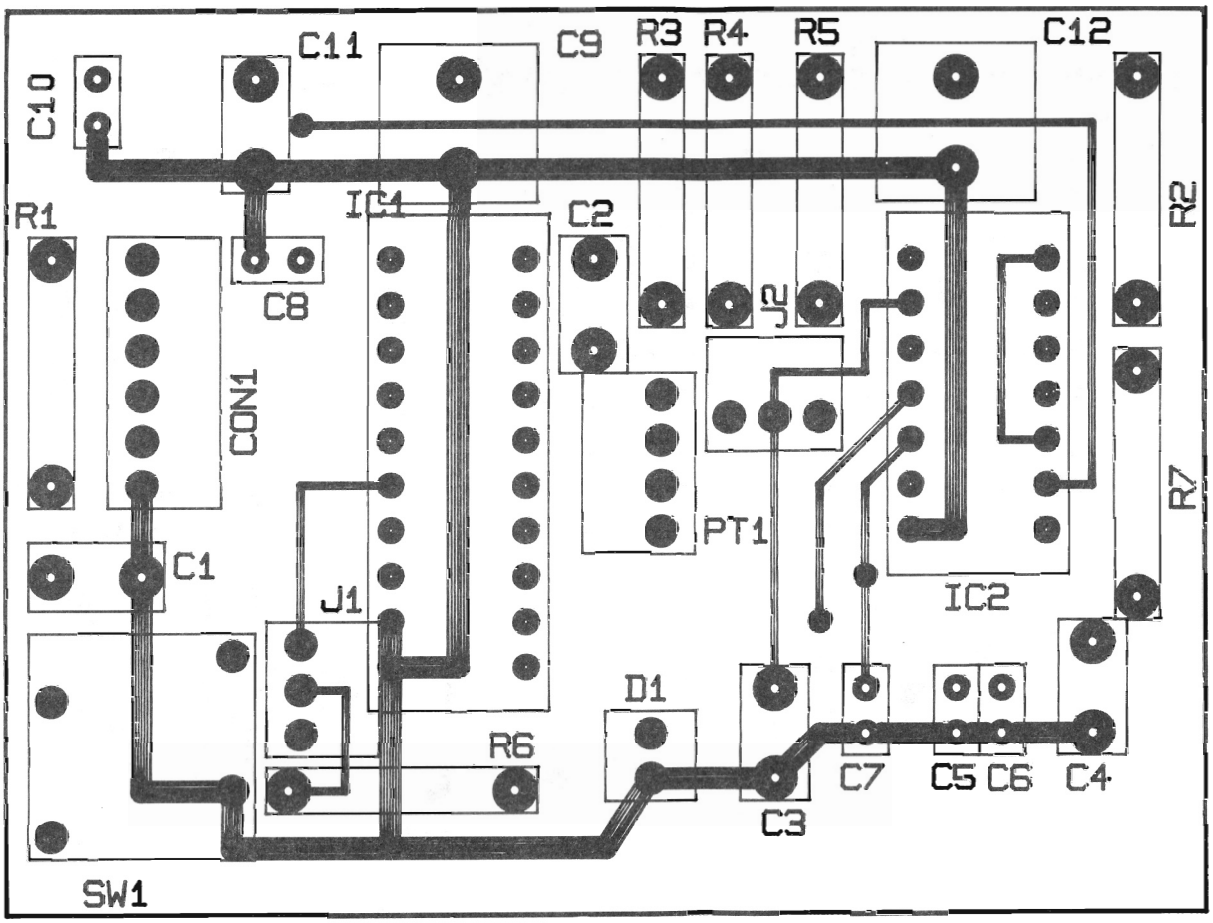

Fig.9 PCB layout (side 2).